System on Chip Seminar

Analog Devices, Inc.

DSP Core Design, Analysis and System Simulation: The ADI Architecture Development Environment

Time to market for any new processor design is as important as ever. However, processor sequencer complexity is increasing. At the same time system simulation requirements are increasing and the number of different system simulation environments is increasing as well. Analog Devices, Inc. has responded to the demands of today's marketplace by building an internal development environment that allows engineering to quickly turn out an entire development-tool-suite. The environment, known as the ADE (architecture development environment) is a set of tools that auto-generates production quality version of an assembler, linker, disassembler, single-line assembler, functional simulator and cycle-accurate simulator. The ADE generated sequencer, when combined with both an existing class library of simulator components and a simulation kernel that supports event-driven simulation semantics, enables ADI to produce cycle-accurate simulators suitable for system simulation in a timely manner. The focus of this presentation will be the ADI ADE environment, the resulting tool chain and the system simulation capabilities of the ADI cycle accurate simulators.

The TigerSHARC DSP for 3G Wireless Infrastructure

ADI is committed to delivering DSP solutions to meet the symbol rate processing requirements of third generation mobile communications systems (3G). This initiative complements a corporate strategy to provide solutions for the entire base station signal chain, including RF technology, high speed converters and digital signal processors. The TigerSHARC DSP addresses the processing requirements of 3G modems with a very high performance and flexible core, a large internal memory, and a powerful DMA controller for managing high bandwidth peripherals. The TigerSHARC also supports flexible system architecture by providing a glueless multiprocessing capability. This capability enables the implementation of processing nodes containing an arbitrary number of gluelessly connected DSPs.

Key features include:

- Efficient implementation of viterbi and turbo decoders
- 14Gbyte/sec internal bus bandwidth and 1.6Gbyte/sec I/O capabilities
- Support of 8Bit, 16Bit, 32Bit fixed or 32Bit floating point data types
- up to 24 16Bit mathematical operations per cycle
- 14 non-intrusive DMA channels with programmable priority and associated interrupts
- 6Mbit of efficiently used internal memory, user definable program and data memory partioning
- Glueless/easy interface to common microprocessors, SDRAM, SRAM, SBSRAM, FPGA's or ASIC's
- Glueless Multiprocessing

GSM Direct Conversion Receiver: The Next Generation Radio

The market demand for smaller and smaller cellular phones continues unabated. Manufacturers must respond with cellular phones that maximize portability, yet include an ever-increasing number of features. This situation has created an ongoing design dilemma for phone OEMs as they struggle to meet consumer demands while continually reducing phone cost and size. Reducing the size and cost of the radio section is now a key area of focus