System on Chip Seminar

Cadence Design Systems

SoC Design Flow: Part 1. IP Authoring

Efficient SoC design requires tested and validated IP blocks, which represent the detailed design of the subsystems used to build the complete SoC. The nature, complexity and functionality of the IP blocks varies a lot. Therefore a wide range of application specific IP authoring tools are required.

Cadence Design Systems provides several IP authoring tools. This presentation introduces the Cierto Signal Processing Worksystem and Affirma Model Packager, which together cover a major part of the communication SoC hardware and DSP.

SoC Design Flow: Part 2. System Integration

When the IP blocks are available, the system functionality and the implementation platform architecture must be put together. The Cierto Virtual Component Codesign (VCC) tool of Cadence Design Systems is a new tool for integrating, analysing and implementing complex HW/SW systems.

This presentation introduces the VCC design methodology and how to use VCC for modeling the functionality of the system, to select an optimal HW platform for it and finally partition and implement the whole chip and automatically generate the communication between the different IP elements.

SoC Design Flow: Part 3. System Verification

Once the SoC is integrated, evaluated and implemented, the final design must be verified. Cadence Design Systems provides a full range of static and dynamic verification tools for SoC verification from system level down to layout verification.

This presentation introduces the System Level verification tools of Cadence Design Systems starting from the formal method and going down to netlist level verification.