SOC 2003
International Symposium on System-on-Chip 2003
19.11.2003 - 21.11.2003
Tampere-Finland

Program Schedule

WEDNESDAY

SESSION WedAmNT1: Opening
09:00 OPENING
Jari Nurmi, *TUT, Finland*

SESSION WedAmOR1: Industry 1
09:30 MOUSTIQUE: SMALLER THAN AN ASIC AND FULLY PROGRAMMABLE
Bernardo Kastrup, Antoine van Wel, *Silicon Hive, Philips Technology Incubator, The Netherlands*

10:00 ACCELERATING SYSTEM PERFORMANCE USING SOPC BUILDER
Brian Dalay, *Altera Europe, UK*

SESSION WedAmOR2: Invited 1
Chair: Jari Nurmi, TUT
10:30 A 2-WAY VLIW PROCESSOR ARCHITECTURE FOR EMBEDDED MULTIMEDIA APPLICATIONS
Wonyong Sung, *Seoul National University, Korea*

11:15 DYNAMIC INSTRUCTION SCHEDULING FOR VLIW - DISVLIW
Kannappan Palaniappan, *University of Missouri, USA*

12:00 LUNCH

SESSION WedPmOR1: Industry 2
13:30 SOC INTEGRATION OF PROGRAMMABLE CORES
Andreas Hoffmann, *CoWare, Germany*

14:00 SOC LOGIC DEVELOPMENT USING CONFIGURABLE, APPLICATION-SPECIFIC PROCESSORS
Chris Rowen, Steven Leibson, *Tensilica, USA*

SESSION WedPmOR2: Invited 2
Chair: Jari Nurmi, TUT
14:30 MULTIPROCESSOR ARCHITECTURE EMPOWERING SYSTEM-ON-CHIP APPLICATIONS
John Goodacre, *ARM, UK*

15:15 MANAGING ON-CHIP COMMUNICATION
Timo D. Hämäläinen, *TUT, Finland*

SESSION WedPmOR3: Industry 3
16:00 A PROGRAMMABLE PLATFORM FOR SOFTWARE-DEFINED RADIO
Hans-Martin Bluethgen, Cyprian Grassmann, Wolfgang Raab, Ulrich Ramacher, *Infineon Technologies AG, Germany*

16:30 XILINX SOLUTIONS FOR INDUSTRIAL AND MEDICAL MARKETS
Giles Peckham, *Xilinx, UK*

SESSION WedPmPS1: Technical Panel: What are the future SoCs made of?
Chair: Jari Nurmi, TUT
17:00

CONFERENCE BANQUET
19:00 Restaurant Finlayson Palace

THURSDAY

SESSION ThuAmOR1: Invited 3
Chair: Jari Nurmi, TUT
09:00 AUTOMATED SIMULATION AND OPTIMIZATION OF MULTI-CORE NPU SOC
William Mangione-Smith, *UCLA, USA*

SESSION ThuAmOR2: Industry 4
09:45 COFFEE - A CORE FOR FREE
Juha Kylliäinen, Jari Nurmi, Mika Kuulusa, *Tampere University of Technology, Finland*

10:10 FUNCTIONAL VERIFICATION FOR NANOMETER SCALE ICS
Riccardo Oddone, *Cadence Design Systems, Italy*

10:35 MENTOR GRAPHICS : CREATE, VERIFY, ANALYZE, OPTIMIZE: THE ROAD TO SOC SUCCESS
Harri Valasma, *Mentor Graphics, Finland*

SESSION ThuAmOR3: Invited 4
Chair: Jari Nurmi, TUT
11:00 ALTERNATIVES TO DSPS - WHAT AND WHY?
Laurent Bonetto, *BDTI, USA*

11:45 PROPERTY-BASED VERIFICATION FOR SOC
Brian Bailey, *Mentor Graphics, USA*

12:30 LUNCH

SESSION ThuPmOR1: SoC/NoC Diversity
13:30 ONE-CHIP SOLUTION IN 0.35 UM STANDARD CMOS FOR ELECTRONIC BALLASTS FOR FLOURESCENT LAMPS
Dirk Killat, Joachim Schmidt, Andreas Baumgaertner, Robert Baraniecki, Oliver Salzmann, *Dialog Semiconductor, Germany*

13:50 EVALUATING APPLICATION MAPPING USING NETWORK SIMULATION
Tommi Salminen, Juha-Pekka Soininen, *VTT Electronics, FINLAND*

14:10 A GUARANTEED-THROUGHPUT SWITCH FOR NETWORK-ON-CHIP
Jian Liu, Li-Rong Zheng, Hannu Tenhunen, *Royal Institute of Technology (KTH), IMIT/LECS, Sweden*

14:30 A CODE COMPRESSION SCHEME FOR IMPROVING SOC PERFORMANCE
Elena Nikolova, David Mulvaney, Vassilios Chouliaras, Jose Nunez-Yanez, *Loughborough University, United Kingdom*

SESSION ThuPmOR2: Industry 5
15:00 AMBA BASED MULTIPROCESSOR SYSTEM
Youngwoo Kim, Kyoung Park, Myungjoon Kim, *ETRI, Korea (South)*

15:30 TESTING SOC DESIGNS WITH CTL
Salvatore Talluto, *Synopsys, Inc., Finland*; Fabienne Desbouvries, *Synopsys, Inc., France*

SESSION ThuPmOR3: SoC applications
16:00 UPDATING MATRIX INVERSE IN FIXED-POINT REPRESENTATION: DIRECT VERSUS ITERATIVE METHODS
Mikko Ylinen, Adrian Burian, Jarmo Takala, *TUT, Finland*

16:20 SOC PLATFORM ARCHITECTURE FOR A NETWORK PROCESSOR
Hany Ghattas, Maria Mbaye, Jean Pepga Bissou, Yvon Savaria, *Ecole Polytechnique Montreal, Canada*

16:40 A LOW POWER DATAPATH FOR ALGEBRAIC CODEBOOK SEARCH TARGETING A GENERIC GSM SYSTEM-ON-CHIP PLATFORM
Antony Kirkham, Tughrul Arslan, *ISLI, UK*; Fred Westall, David Crawford, *EPSON SDC, UK*

17:00 COMPLEXITY ANALYSIS OF SPATIALLY SCALABLE MPEG-4 ENCODER
Olli Lehtoranta, Timo Hämäläinen, *Tampere University of Technology/Institute of Digital and Computer Systems, Finland*

Ice Hockey Session
18:30 Tappara - TPS

Supper
21:00 Restaurant Plevna

FRIDAY

SESSION FriAmOR1: Invited 5
Chair: Jari Nurmi, TUT
09:00 THE ARCHITECTURAL CHALLENGE OF NEXT GENERATION COMMUNICATION SYSTEMS
Ulrich Ramacher, *Infineon Technologies, Germany*

SESSION FriAmPS1: Policy Panel: Success factors for future SoC research and education strategies
Chair: Jari Nurmi, TUT
09:45

SESSION FriAmOR2: Configurable and reconfigurable hardware
11:15 IMPLEMENTING USER AND APPLICATION SPECIFIC ALGORITHMS WITHIN IP-METHODOLOGY: A COARSE-GRAIN-APPROACH
Tapio Ristimäki, Jari Nurmi, *Tampere University of Technology, Finland*

11:35 IMMEDIATE OPTIMIZATION FOR COMPRESSED TRANSPORT TRIGGERED ARCHITECTURE INSTRUCTIONS
Jari Heikkinen, Tommi Rantanen, Andrea Cilio, Jarmo Takala, *Tampere University of Technology, Finland*; Henk Corporaal, *Eindhoven University of Technology, The Netherlands*

11:55 A C-BASED ALGORITHM DEVELOPMENT FLOW FOR A RECONFIGURABLE PROCESSOR ARCHITECTURE
Claudio Mucci, Carlo Chiesa, Andrea Lodi, Mario Toma, Fabio Campi, *ARCES - University of Bologna, Italy*

12:15 XICU – AN INTERRUPT CONTROL UNIT FOR A CONFIGURABLE DSP CORE
Christian Panis, *Carinthian Tech Institute, Austria*; Johannes Hohl, *Infineon Technologies, Austria*; Herbert Grünbacher, *Carinthian Tech Institute, Austria*; Jari Nurmi, *Tampere University of Technology, Finland*

SESSION FriAmOR3: Interconnects
11:15 HIGHLY SCALABLE NETWORK ON CHIP FOR RECONFIGURABLE SYSTEMS
Andrei Bartic, Jean-Yves Mignolet, Vincent Nollet, Theodore Marescaux, Diederik Verkest, Serge Vernalde, Rudy Lauwereins, *IMEC, Belgium*

11:35 A HIGLY EFFICIENT MODELING STYLE FOR HETEROGENEOUS BUS ARCHITECTURES
Manoj Ariyamparambath, *Sysnopsys Inc., INDIA*; Denis Bussaglia, *Synopsys Inc., FRANCE*; Bernd Reinkemeier, *Synopsys Inc, GERMANY*; Tim Kogel, Torsten Kempf, *Integrated Signal Processing Systems, Aachen University, GERMANY*

11:55 MODELING ON-CHIP COMMUNICATION
Tiberiu Seceleanu, *Univ.ersity of Turku, Finland*; Juha Plosila, *Univ. of Turku, Finland*

12:15 TWISTED DIFFERENTIAL ON-CHIP INTERCONNECT ARCHITECTURE FOR INDUCTIVE/CAPACITIVE CROSSTALK NOISE CANCELLATION
Ilhan Hatirnaz, Yusuf Leblebici, *Swiss Federal Institute of Technology (EPFL), Switzerland*

12:35 LUNCH

SESSION FriPmPO1: Poster 1
14:00

DYNAMIC CLAMPING: ON-CHIP DYNAMIC SHIELDING AND TERMINATION FOR HIGH-SPEED RLC BUSES
Kanak Agarwal, Dennis Sylvester, David Blaauw, *University of Michigan, USA*

A DRIVER LOAD MODEL FOR CAPACITIVE COUPLED ON-CHIP INTERCONNECT BUSES
Markus Tahedl, Hans-Jörg Pfleiderer, *University of Ulm, Department of Microelectronics, Germany*

USING A COMMUNICATION GENERATOR IN SOC ARCHITECTURE EXPLORATION
Tero Kangas, Jouni Riihimäki, Erno Salminen, Kimmo Kuusilinna, Timo Hämäläinen, *Tampere University of Technology, Finland*

ARITHMETIC PROCESSING UNIT FOR RECIPROCAL OPERATIONS
Kim Rounioja, Jari Parviainen, *Nokia Mobile Phones, Finland*

NEW ADAPTIVE ROUTING ALGORITHM FOR EXTENDED GENERALIZED FAT TREES ON-CHIP
Heikki Kariniemi, Jari Nurmi, *Institute of Digital and Computer Systems, Tampere University of Technology, Finland*

MAPPABILITY ESTIMATE: A MEASURE OF THE GOODNESS OF A PROCESSOR-ALGORITHM PAIR
Jari Kreku, Juha-Pekka Soininen, *VTT Electronics, Finland*

MULTIPLE-OBJECTIVE BACKTRACE FOR SOLVING TEST GENERATION CONSTRAINTS
Jaan Raik, Andrei Mekler, *Tallinn Technical University, Estonia*

A SYSTEM LEVEL IP INTEGRATION METHODOLOGY FOR FAST SOC DESIGN
Massimo Bocchi, *ARCES - University of Bologna, Italy*; Claudio Brunelli, *Tampere University of Technology, Finland*; Claudia De Bartolomeis, Luca Magagni, Fabio Campi, *ARCES - University of Bologna, Italy*

VLIW OPERATION REFINEMENT FOR REDUCING ENERGY CONSUMPTION
Ulrich Hirnschrott, Andreas Krall, *TU Wien, Austria*

A DELAY SPREAD BASED LOW POWER RECONFIGURABLE FFT PROCESSOR ARCHITECTURE FOR WIRELESS RECEIVERS
Mohammad Hasan, *School of Engineering and Electronics, University of Edinburgh, India*; Tughrul Arslan, John Thompson, *School of Engineering and Electronics,University of Edinburgh, U.K.*

DESIGN OF A PARAMETRIZABLE LOW COST ETHERNET MAC CORE FOR SOC SOLUTIONS
Jose Antonio Moreno Zamora, Pedro Jose Rodriguez Corrales, Juan Manuel Sanchez Perez, *University of Extremadura, Spain*

LOOPBACK BIST FOR RF FRONT-ENDS IN DIGITAL TRANSCEIVERS
Jerzy Dabrowski, *Linkoping University, Sweden*

ABSTRACT RTOS MODELLING FOR MULTIPROCESSOR SYSTEM-ON-CHIP
Jan Madsen, Kashif Virk, Mercury Gonzales, *Technical University of Denmark, Denmark*

ANALYSIS AND DESIGN OF LEVEL-CONVERTING FLIP-FLOPS FOR DUAL-VDD/VTH INTEGRATED CIRCUITS
Robert Bai, Dennis Sylvester, *University of Michigan at Ann Arbor, USA*

EVALUATION OF FULLY-INTEGRATED SWITCHING REGULATORS FOR CMOS PROCESS TECHNOLOGIES
Jaeseo Lee, *University of California, Los Angeles, U.S.A.*; Geoff Hatcher, *Conexant Corp., U.S.A.*; Lieven Vandenbergh, Chih-Kong Ken Yang, *University of California, Los Angeles, U.S.A.*

MIXED STATIC/DYNAMIC PROFILING FOR DICTIONARY BASED CODE COMPRESSION
Eduardo Netto, *CEFET-RN / IC-UNICAMP, Brasil*; Rodolfo Azevedo, Paulo Centoducatte, Guido Araujo, *IC-UNICAMP, Brazil*

AVISPA: A MASSIVELY PARALLEL RECONFIGURABLE ACCELERATOR
Jeroen Leijten, Geoffrey Burns, Jos Huisken, Erwin Waterlander, Antoine van Wel, *Silicon Hive, The Netherlands*

SESSION FriPmOR1: Invited 6
Chair: Jari Nurmi, TUT
15:30 DYNAMICALLY RECONFIGURABLE PROCESSOR
Masato Motomura, *NEC, Japan*

SESSION FriPmNT1: Closing
16:15 - 16:30 CLOSING
Jari Nurmi, *TUT, Finland*