SOC 2003
International Symposium on System-on-Chip 2004
16.11.2004 - 18.11.2004
Tampere-Finland

NOTE! All industry and poster sessions in Hall B, all other sessions in Studio.

Program Schedule

Advanced Program as of October 25, 2004

TUESDAY

SESSION TueAmOR1: Opening

09:30 WELCOME TO SOC 2004
Jari Nurmi, TUT, Finland

SESSION TueAmOR2: Keynote
Chair: Jari Nurmi, TUT, Finland

09:45 APPLICATION SPECIFIC INSTRUCTION-SET PROCESSORS (ASIP'S) FOR WIRELESS COMMUNICATIONS:
DESIGN, COST, AND ENERGY EFFICIENCY VS. FLEXIBILITY
Heinrich Meyr, RWTH Aachen, Germany

SESSION TueAmOR3: Industry 1
non-chaired

10:30 IMPLEMENTING A SINGLE-PROCESSOR CELLULAR MODEM ON AN SC1000-FAMILY CORE
Stefano Angioni, StarCore LLC, Germany; Floyd Lazare, TTPCom Ltd., UK

11:00 A HIGH LINEARITY ANALOG FRONT END FOR MULTIPROCESSOR SOC INTEGRATION
Yong Luo, Agere Systems, USA

SESSION TueAmOR4: Invited 1
Chair: Jari Nurmi, TUT, Finland
11:30 OPTIMIZING A HIGH PERFORMANCE 32-BIT PROCESSOR FOR PROGRAMMABLE LOGIC
Paul Metzgen, Altera, UK

12:15 LUNCH

SESSION TuePmOR1: Industry 2
non-chaired

13:30 SPIDERGON: A NOVEL ON-CHIP COMMUNICATION NETWORK
Marcello Coppola, Locatelli Riccardo, Maruccia Giuseppe, Pieralisi Lorenzo, STM, France;
Scandurra Alberto, STM, Italy

14:00 RAPID HARDWARE CREATION USING UNTIMED C++ SYNTHESIS
Håkan Pettersson, Mentor Graphics,

SESSION TuePmOR2: Invited 2
Chair: Jari Nurmi, TUT, Finland

14:30 CIRCUITS WITHOUT CLOCKS: WHAT MAKES THEM TICK?
Jo Ebergen, Sun Microsystems, USA

SESSION TuePmOR3: Industry 3
non-chaired

15:15 t.b.d., Infineon, Germany

15:45 t.b.d., Atmel, Finland

SESSION TuePmOR4: Routing HW for NoC
Chair: Harri Lampinen, TUT, Finland

16:15 GLOBAL ROUTING FOR MULTICAST-SUPPORTING TDM NETWORK-ON-CHIP
Jian Liu, Li-Rong Zheng, Hannu Tenhunen, Royal Institute of Technology (KTH), Sweden

16:35 FLIT ADMISSION IN ON-CHIP WORMHOLE-SWITCHED NETWORKS WITH VIRTUAL CHANNELS
Zhonghai Lu, Axel Jantsch, Royal Institute of Technology, Sweden

16:55 DESIGN OF A GUARANTEED THROUGHPUT ROUTER FOR ON-CHIP NETWORKS
Sumant Sathe, Daniel Wiklund, Dake Liu, Linköpings universitet, Sweden

SESSION TuePmNT1: Snack and Drinks

17:15 – 19:00 Informal get-together in the exhibit hall (Hall B)

WEDNESDAY

SESSION WedAmOR1: Networks on Chip
Chair: Tapani Ahonen, TUT, Finland

09:00 LESSONS LEARNED FROM DESIGNING THE MONTIUM
Gerard Smit, Paul Heysters, Michel Rosien, Bert Molenkamp, University of Twente, Netherlands

09:20 EFFICIENT BARRIER SYNCHRONIZATION MECHANISM FOR EMULATED SHARED MEMORY NOCS
Martti Forsell, VTT Electronics, Finland

09:40 PROVIDING QOS TO CONNECTION-LESS PACKET-SWITCHED NOC BY IMPLEMENTING DIFFSERV FUNCTIONALITIES
Mehmet Derin Harmanci, LAP - EPFL, Switzerland; Nuria Pazos, LAP/LSM - EPFL, Switzerland;
Yusuf Leblebici, LSM-EPFL, Switzerland; Paolo Ienne, LAP - EPFL, Switzerland

SESSION WedAmOR2: Industry 4
non-chaired

10:00 INCREASE DESIGNER PRODUCTIVITY AND REDUCE DESIGN RISKS THROUGH PROCESSOR-CENTRIC SOC DESIGN
Steve Leibson, Tensilica, USA

10:30 t.b.d.

SESSION WedAmOR3: Invited 3
Chair: Jari Nurmi, TUT, Finland

11:00 STREAM ARCHITECTURES - EFFICIENCY AND PROGRAMMABILITY
Mattan Erez, Stanford University, USA

SESSION WedAmOR4: System-Level Issues
Chair: Jouni Tomberg, TUT, Finland

11:45 EVALUATION OF PLATFORM ARCHITECTURE PERFORMANCE USING ABSTRACT INSTRUCTION-LEVEL WORKLOAD MODELS

Jari Kreku, Tarja Kauppi, Juha-Pekka Soininen, VTT Electronics, Finland

12:05 PRACTICAL DISTRIBUTED SIMULATION OF A NETWORK OF WIRELESS TERMINALS
Jouni Riihimäki, Petri Kukkala, Erno Salminen, Marko Hännikäinen, Kimmo Kuusilinna,
Timo Hämäläinen, Tampere University of Technology, Finland

12:25 A MODEL FOR IMAGING SYSTEM-ON-CHIP MANUFACTURING COSTS
Cade Wells, Institute for System Level Integration, UK; Ed Duncan, STMicroelectronics, UK;
David Renshaw, University of Edinburgh, UK

12:45 LUNCH

SESSION WedPmOR1: Industry 5
non-chaired

14:00 t.b.d.

14:30 t.b.d.

SESSION WedPmOR2: Blocks for SoC
Chair: Marko Hännikäinen, TUT, Finland

15:00 A LOW-NOISE FAST-SETTLING PLL FREQUENCY SYNTHESIZER FOR CDMA RECEIVERS
Shaojun Wu, Dalhousie University, Canada

15:20 A LOW-POWER I-CACHE DESIGN WITH TAG-COMPARISON REUSE
Koji Inoue, Hidekazu Tanaka, Vasily Moshnyaga, Fukuoka Univ., Japan;
Kazuaki Murakami, Kyusyu Univ., Japan

15:40 COMPARISON OF HARDWARE IP COMPONENTS FOR SYSTEM-ON-CHIP
Erno Salminen, Kimmo Kuusilinna, Timo Hämäläinen, TUT / DCS, Finland

SESSION WedPmOR3: Invited 4
Chair: Jari Nurmi, TUT, Finland

16:00 REDUCTION OF DESIGN COMPLEXITY USING VIRTUAL HARDWARE PLATFORMS
Tero Rissa, Imperial College, UK

SESSION WedPmNT1: Coffee
Sponsor: Infineon Technologies

16:45 – 17:00 Exceptionally in front of Studio

SESSION WedPmPS1: Panel discussion

17:00 – 18:30 “Processors for SoC – what, why and how?”

SESSION WedPmNT2: Banquet in Finlayson Palace

19:00 – 22:00 Three-course banquet

THURSDAY

SESSION ThuAmOR1: SoC-Mobinet Special Session
Organizer: SoC-Mobinet
Chair: Jan Madsen, Technical University of Denmark, Denmark

09:00 SOC-MOBINET, R&D AND EDUCATION IN SYSTEM-ON-CHIP DESIGN
Erwin Ofner, CTI, Austria; Jari Nurmi, TUT, Finland; Jan Madsen, DTU, Denmark;
Jouni Isoaho, UTU, Finland; Hannu Tenhunen, KTH, Sweden

09:30 A SYSTEM-LEVEL MULTIPROCESSOR SYSTEM-ON-CHIP MODELING FRAMEWORK
Kashif Virk, Jan Madsen, Technical University of Denmark, Denmark

09:50 A SCALABLE EMBEDDED DSP CORE FOR SOC APPLICATIONS
Christian Panis, Carinthian Tech Institute, Austria; Ulrich Hirnschrott, Stefan Farfeleder,
Andreas Krall, Vienna University of Technology, Austria; Gunther Laure, Wolfgang Lazian,
Infineon Technologies Austria, Austria; Jari Nurmi, Tampere University of Technology, Finland

10:10 ANALYSES OF SIGNALING TECHNIQUES FOR SELF-TIMED SYSTEMS
Ethiopia Nigussie, Johanna Tuominen, Jouni Isoaho, University of Turku, Finland

10:30 SOC-MOBINET: BROADBAND TRANSCEIVER DESIGN CHALLENGES
Franz Dielacher, Infineon Technologies, Austria

SESSION ThuAmPO1: Poster Session: SoC-Mobinet and Related Work
Organizer: SoC-Mobinet
non-chaired

11:00 REUSABLE XGFT INTERCONNECT IP FOR NETWORK-ON-CHIP IMPLEMENTATIONS
Heikki Kariniemi, Jari Nurmi, Tampere University of Technology, Finland

11:00 A RECONFIGURABLE FPU AS IP COMPONENT FOR SOCS
Claudio Brunelli, Tampere University of Technology, Finland; Fabio Campi,
ARCES Laboratories - University of Bologna, Italy; Juha Kylliäinen, Jari Nurmi,
Tampere University of Technology, Finland

11:00 VERIFICATION OF A 32-BIT RISC PROCESSOR CORE
Tuukka Kasanko, Jari Nurmi, Tampere University of Technology, Finland

11:00 CONFIGURABLE COMPUTING ARCHITECTURES FOR WIRELESS AND SOFTWARE DEFINED RADIO -
A FPGA PROTOTYPING EXPERIENCE USING HIGH LEVEL DESIGN-TOOL-CHAINS -
Alfred Blaickner, Carinthia Tech Institute - CTI, Austria; Susanne Albl, CTI, Austria;
Wolfgang Scherr, Infineon, Austria

11:00 RECONFIGURABLE IP BLOCKS : A SURVEY
Tapio Ristimäki, Jari Nurmi, Institute of Digital and Computer Systems,
Tampere University of Technology, Finland

11:00 A SYNTHESIZABLE RTL DESIGN OF ASYNCHRONOUS FIFO
Xin Wang, Tapani Ahonen, Jari Nurmi, Institute of Digital and Computer Systems,
Tampere University of Technology, Finland

11:00 DESIGN REUSE AND DESIGN FOR REUSE, A CASE STUDY ON HDSL2
Tapani Ahonen, Jari Nurmi, Tampere University of Technology, Finland

11:00 TOPOLOGY DESIGN FOR GLOBAL LINK OPTIMIZATION IN APPLICATION SPECIFIC NETWORK-ON-CHIPS
David A. Sigüenza-Tortosa, Jari Nurmi, DCS-TUT, Finland

11:00 CROSSTALK IMMUNE INTERCONNECT DRIVER DESIGN
Roshan Weerasekera, Li-Rong Zheng, KTH/IMIT/LECS, Sweden; Dinesh Pamunuwa,
Lancaster University, UK; Hannu Tenhunen, KTH/IMIT/LECS, Sweden

11:00 HARDWARE UNIT FOR OVSF/WALSH/HADAMARD CODE GENERATION
Timo Rintakoski, Tampere University of Technology, Finland; Mika Kuulusa, Nokia, Finland;
Jari Nurmi, Tampere University of Technology, Finland

SESSION ThuPmOR1: Invited 5
Chair: Jari Nurmi, TUT, Finland

12:00 DEVELOPMENT OF NSOC PROGRAM IN TAIWAN
Chun-Yen Chang, NCTU, Taiwan

SESSION ThuPmOR2: IEE award winner session
Chair: Jari Nurmi, TUT, Finland

12:45 A SYSTEM-ON-A-CHIP FOR AUDIO ENCODING
Jacob Bower, Imperial College, UK

13:05 LUNCH

SESSION ThuPmPO1: Poster Session
non-chaired

14:00 EC-A COMPILER FOR THE E-LANGUAGE
Martti Forsell, VTT Electronics, Finland

14:00 ESTIMATION OF A MAXIMUM BOUND OF UNCERTAIN PARAMETER FLUCTUATIONS WITH APPLICATIONS TO ANALOGUE IP-CORES
HJ Kadim, Liverpool JM University, United Kingdom

14:00 EFFICIENT TILE-AWARE BOUNDING-BOX OVERLAP TEST FOR TILE-BASED RENDERING
Iosif Antochi, Ben Juurlink, Stamatis Vassiliadis, Delft University of Technology,
The Netherlands; Petri Liuha, Nokia Research Center, Finland

14:00 SCALABILITY ANALYSIS OF EVOLVING SOC INTERCONNECT PROTOCOLS
Martino Ruggiero, Federico Angiolini, Francesco Poletti, Davide Bertozzi, Luca Benini,
DEIS - Università di Bologna, Italy; Roberto Zafalon, STMicroelectronics, Italy

14:00 HIGH SPEED AND LOW POWER ON-CHIP MICRO NETWORK CIRCUIT WITH DIFFERENTIAL TRANSMISSION LINE
Shinichiro Gomi, Kohichi Nakamura, Hiroyuki Ito, Hideyuki Sugita, Kenichi Okada, Kazuya Masu, Tokyo Institute of Technology, Japan

14:00 ASSERTION BASED VERIFICATION OF PSL FOR SYSTEMC DESIGNS
Ali Habibi, Amjad Gawanmeh, Sofiene Tahar, Concordia U., Canada

14:00 A THERMAL-AWARE POWER MANAGEMENT SOFT-IP FOR PLATFORM-BASED SOC DESIGNS
Chinhung Chang, Yucheng Chang, Hsichi Ho, Herming Chiueh, National Chiao Tung University, Taiwan

14:00 COMPARATIVE ANALYSIS OF SERIAL VS PARALLEL LINKS IN NOC
Arkadiy Morgenshtein, Israel Cidon, Avinoam Kolodny, Ran Ginosar, Technion, Israel Institute of Technology, EE Department, Israel

14:00 A FULLY INTEGRATED LOW-IF DVB-T RECEIVER ARCHITECTURE
Goran Andrijevic, Håkan Magnusson, Håkan Olsson, KTH, SWEDEN

14:00 AN IN-CIRCUIT DEBUG ENVIRONMENT FOR MULTIPROCESSOR SOCS BASED ON A HDL RISC SOFT-CORE
Roberto Pelliconi, ST Microelectronics, Italy; Fabio Campi, ARCES,
University of Bologna, Italy; Lorenzo Salsa, STMicroelectronics, Italy; Claudio Mucci,
Stefano Macchiavelli, ARCES, University of Bologna, Italy

14:00 REFINEMENT OF ON-CHIP COMMUNICATION CHANNELS
Juha Plosila, Pasi Liljeberg, Jouni Isoaho, University of Turku, Finland

14:00 DESIGN FOR VERIFICATION OF A PCI BUS IN SYSTEMC
Karim Oumalou, Ali Habibi, Sofiene Tahar, Concordia U., Canada

SESSION ThuPmOR3: Invited 6
Chair: Jari Nurmi, TUT, Finland

15:00 3D GRAPHICS CIRCUITS FOR 3G MULTIMEDIA TERMINALS
Ramchan Woo, KAIST, Korea

15:45 CLOCK GENERATION AND DISTRIBUTION IN HIGH-PERFORMANCE PROCESSORS
Stefan Rusu, Intel, USA

SESSION ThuPmOR4: Closing

16:30 GOODBYE
Jari Nurmi, TUT, Tampere "The SoC City", Finland

SESSION ThuPmNT1: Ice-Hockey Ilves vs. Blues
Sponsor: Mentor Graphics

18:30 The game starts in the oldest ice hall in Finland

SESSION ThuPmNT2: Supper in Restaurant Plevna
Sponsor: Tampere University of Technology

21:00 – 23:00 Food and beer served. Our warmest goodbye.