SoC-MOBINET

KTH

SoC-Mobinet, R&D and Education in SoC Design

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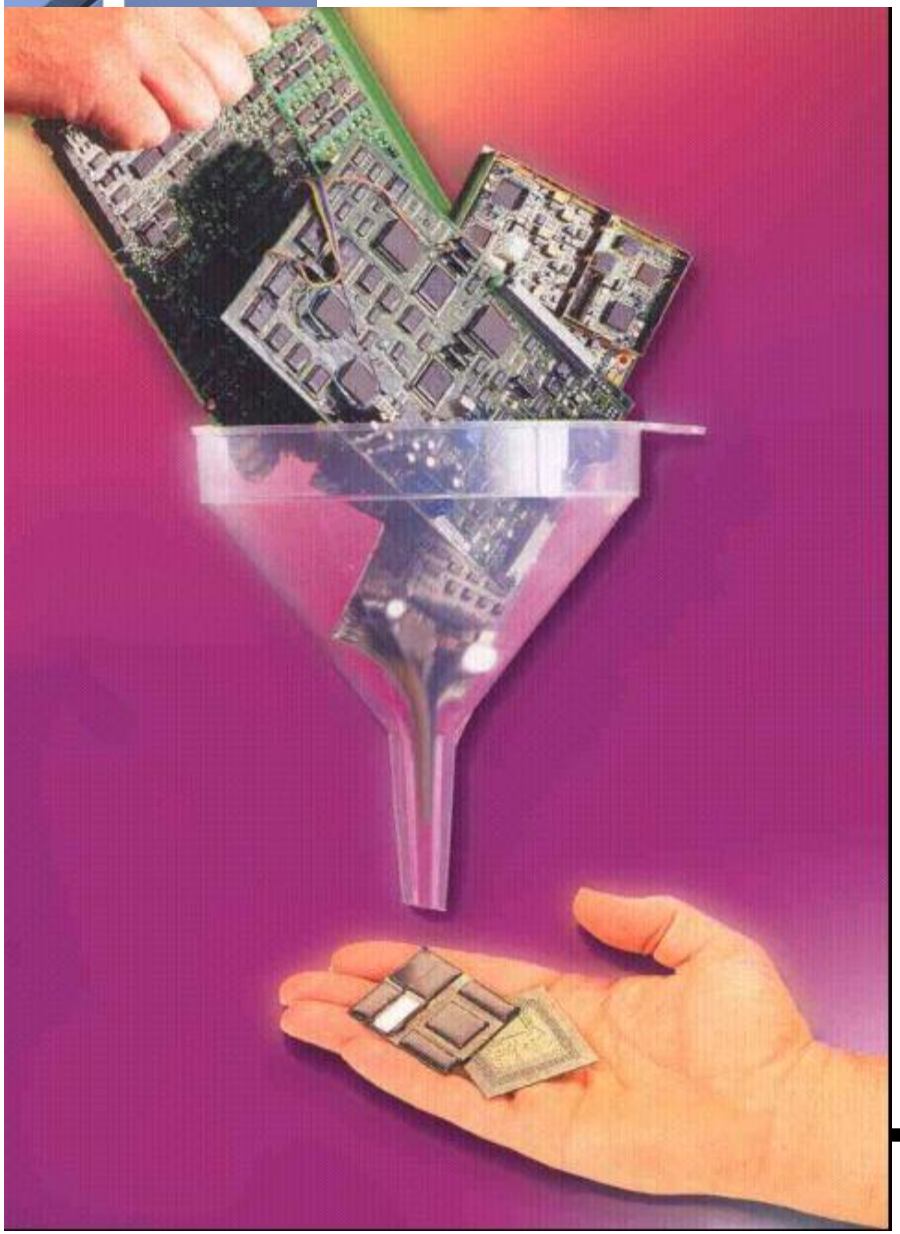
Outline

- Challenges in SoC design
- SoC-mobinet project and key results
- Future research& education activities

SoC: At the Heart of Conflicting Trends



Time-to-Market Pressure:

Process roadmap acceleration
Consumerization of electronic devices
IP-Reuse? SoC versus SoP?

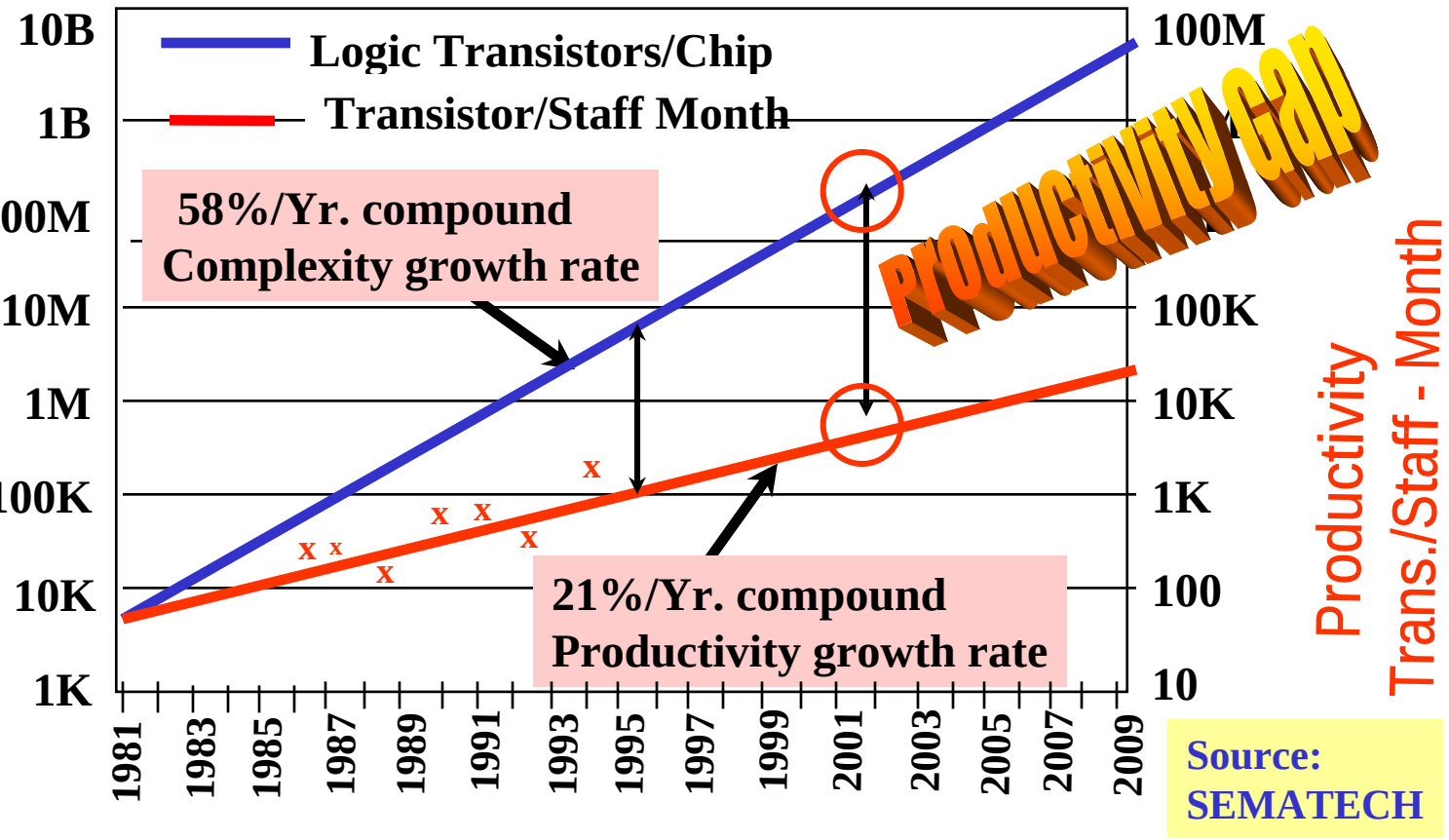
Design Complexity:

uP, DSP, HW/SW, RTOS
SW Protocol Stacks
Digital/Analog IPs, Mixed-Signal Integration?
On-Chip Bus, Standard IP Interface?
IP-based design, SoC Platform ?

Deep Submicron Effects:

Crosstalk, Electromigration
Interconnect Delay, Power Supply noise
Timing closure? New design flow?

The Productivity Gap



- 100M logic gates in 90nm = Logic of 1000 ARM7's
- Current 0.13u SoC's: 10M$ ~100M$ design cost

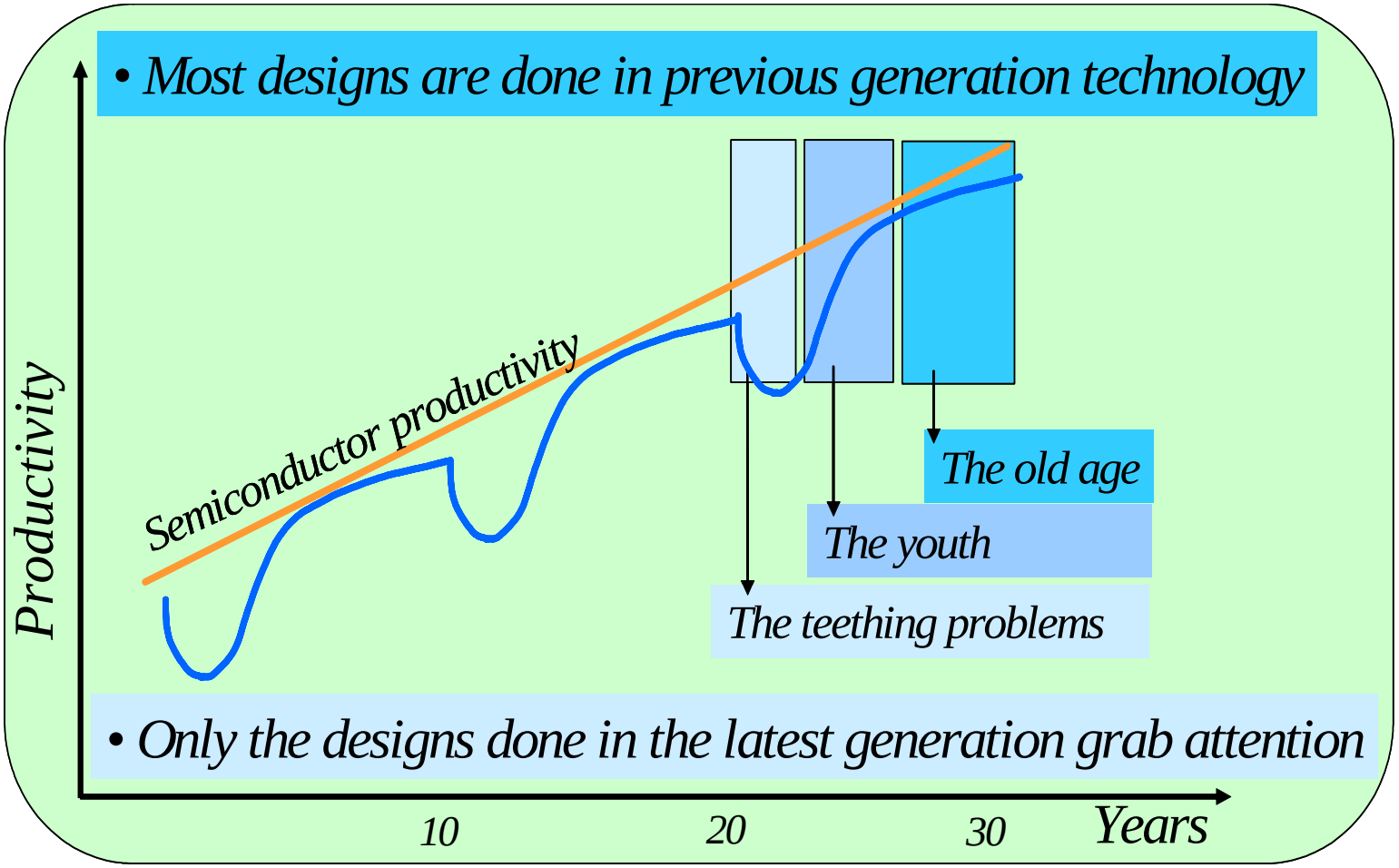
Kiss of death

ASIC, as understood in 1990's, is dead!
VLSI was dead already in 1990s!
SoC is dead already in 2004
Platforms and NoC may not work out towards end of this decade; only very few mainstream applications where NoC will take over

Most of the curriculums are still either VLSI or ASIC centric

Open source platforms and technologies may change all of this

The productivity gap is a myth



Hemani's Conjecture

Moore's law over a decade $2^{10/1.5} \approx 100$

Complexity of reusable objects increases by two order of magnitude every decade.

- Ahmed Hemani 1998

2013	***Sub systems***	***10^6 X***
2003	***Algorithms / IP blocks***	***10^4 X***
1993	***Computational units***	***10^2 X***
1983	***Gates, Flip Flops etc.***	***X***

NoC is a Plausible Next Step

Algorithm on a Chip

Work in 1980s on VLSI, DSP-ASIC, silicon compilation, layout genrators, design libraries
Transistor/gate centric

Hardwired Computation

Hardwired Communication

System on a Chip

Work in 1990s. Synthesis centric research, Core processors, busses, reusability
Low power. Interconenct centric

Programmable Computation

Hardwired Communication

Network on a Chip

Communicaton centric

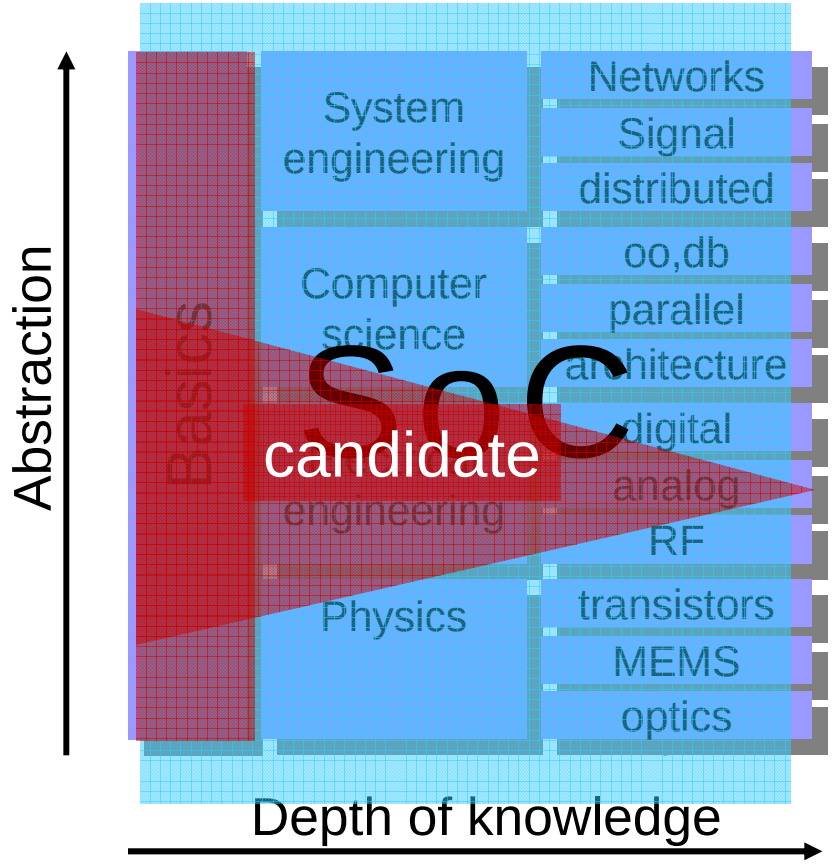
Programmable Computation

Programmable Communication

Design technology nodes

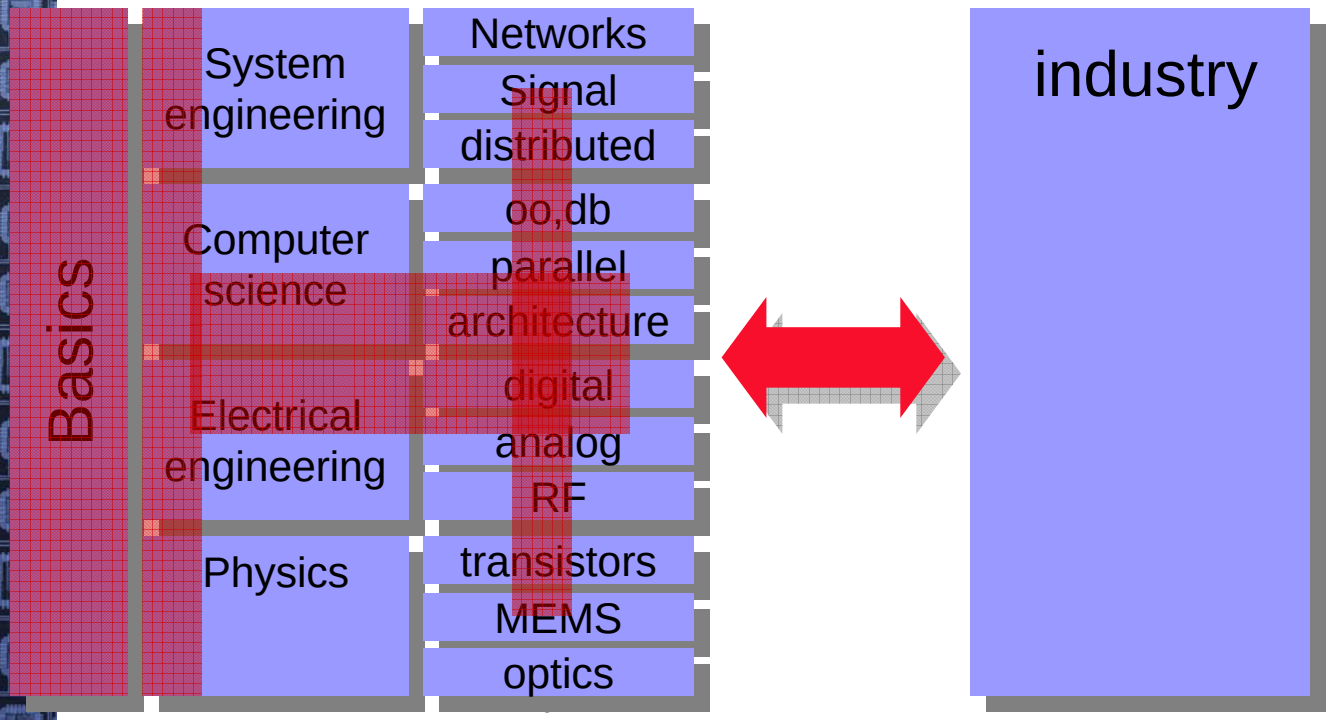
Decade	Design Technology Node	Design Element	Granularity	Chip Architecture
2010s	Communication centric Platform Based Design	Sub-systems, Commn. Centric Platforms	10^6 X	Network on a chip
2000s	IP/Processor Centric Platform based design	IPs e.g. RISC/DSP cores, USB, DSP functions	10^4 X	System on a chip
1990s	RTL/ Logic Synthesis	RTL Objects e.g., arithmetic units, registers, multiplexors	10^2 X	Algorithm on a chip
1980s	Physical Synthesis	Std. Cells, e.g., Logic gates, flops, latches	X	
1970s	Manual	Polygons		

SoC program structures: Current form



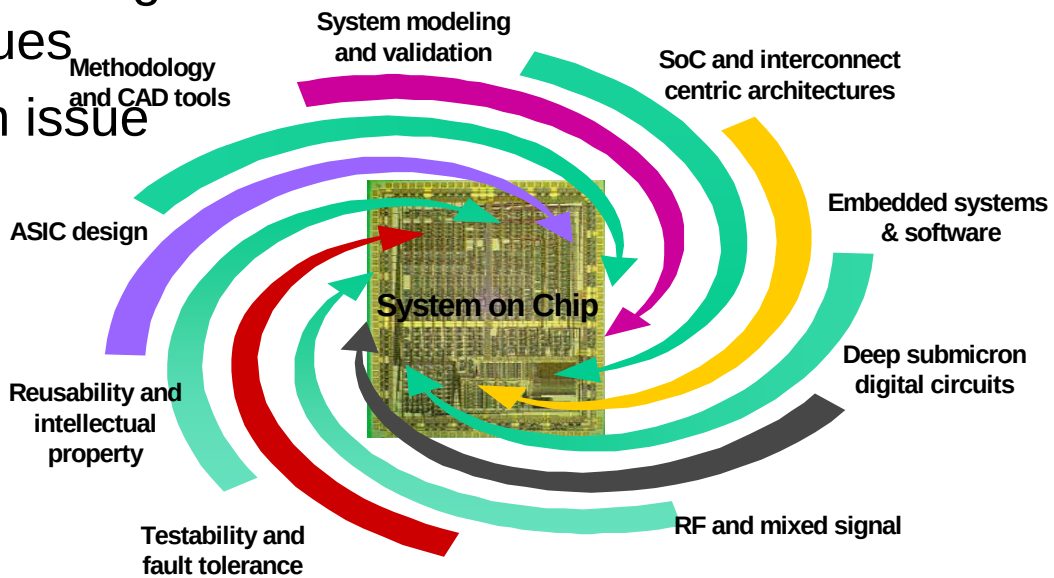
the SoC dilemma!

SoC directions



Tenhunen's Conjecture

- Number of courses needed for training IC/VLSI/SOC designers will double per decade
  - Indicates a serious lack of abstractions and deeper understanding of fudamental issues
  - Interfaces open issue and problem
- Not sustainable



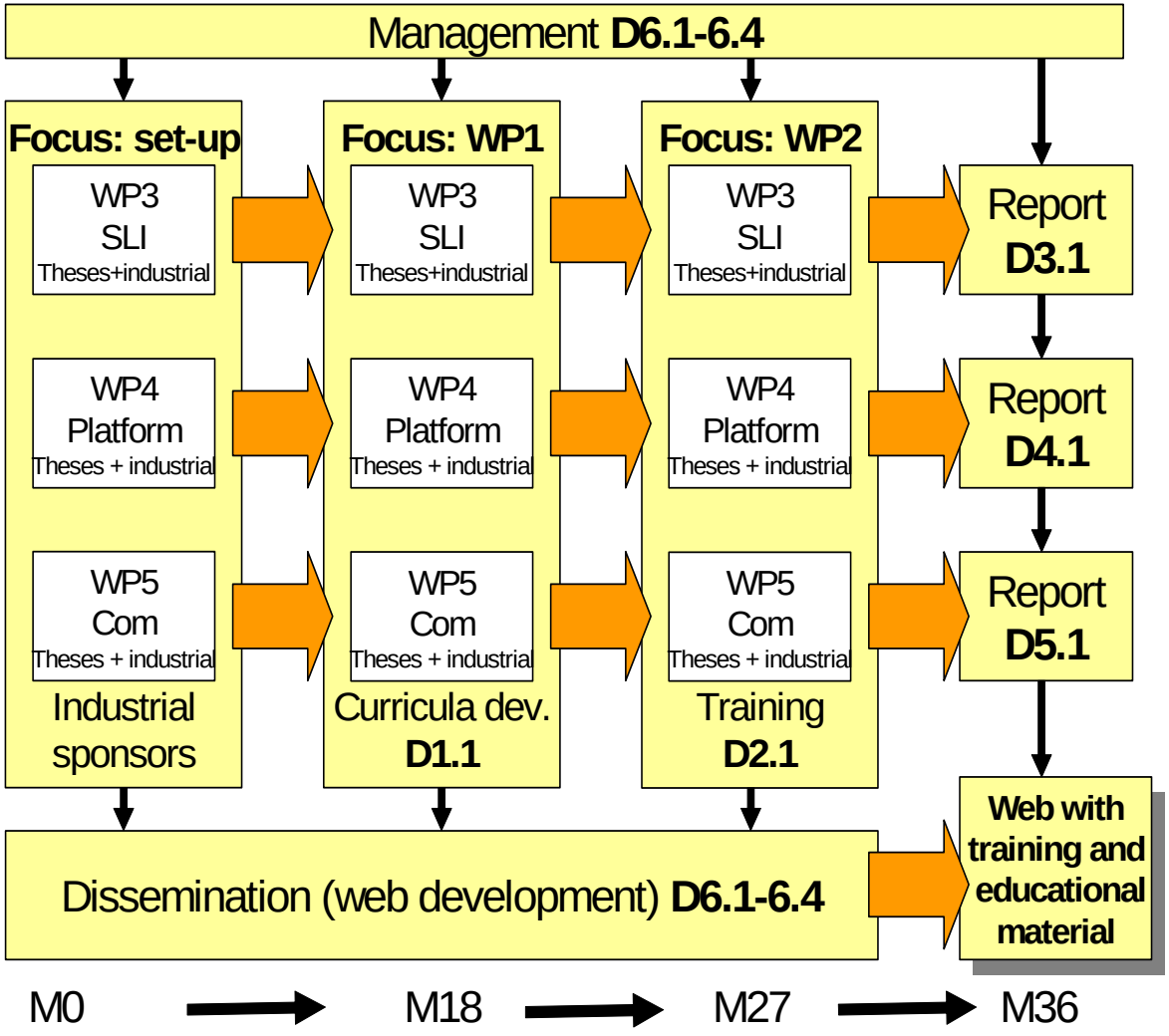
Challenges

- Design efficiency and quality improvements.
- Heterogeneous ASICs (multiple DSP and RISC core processors, embedded SW, higher design abstraction, synthesis techniques).
- Reusability, resulting to more efficient IP encapsulation.
- Design optimization strategies
- Chip and system level synchronization strategies
- Low power design strategies
- Codesign.
- Mixed signal design strategies.
- Internationalization
- Bologna

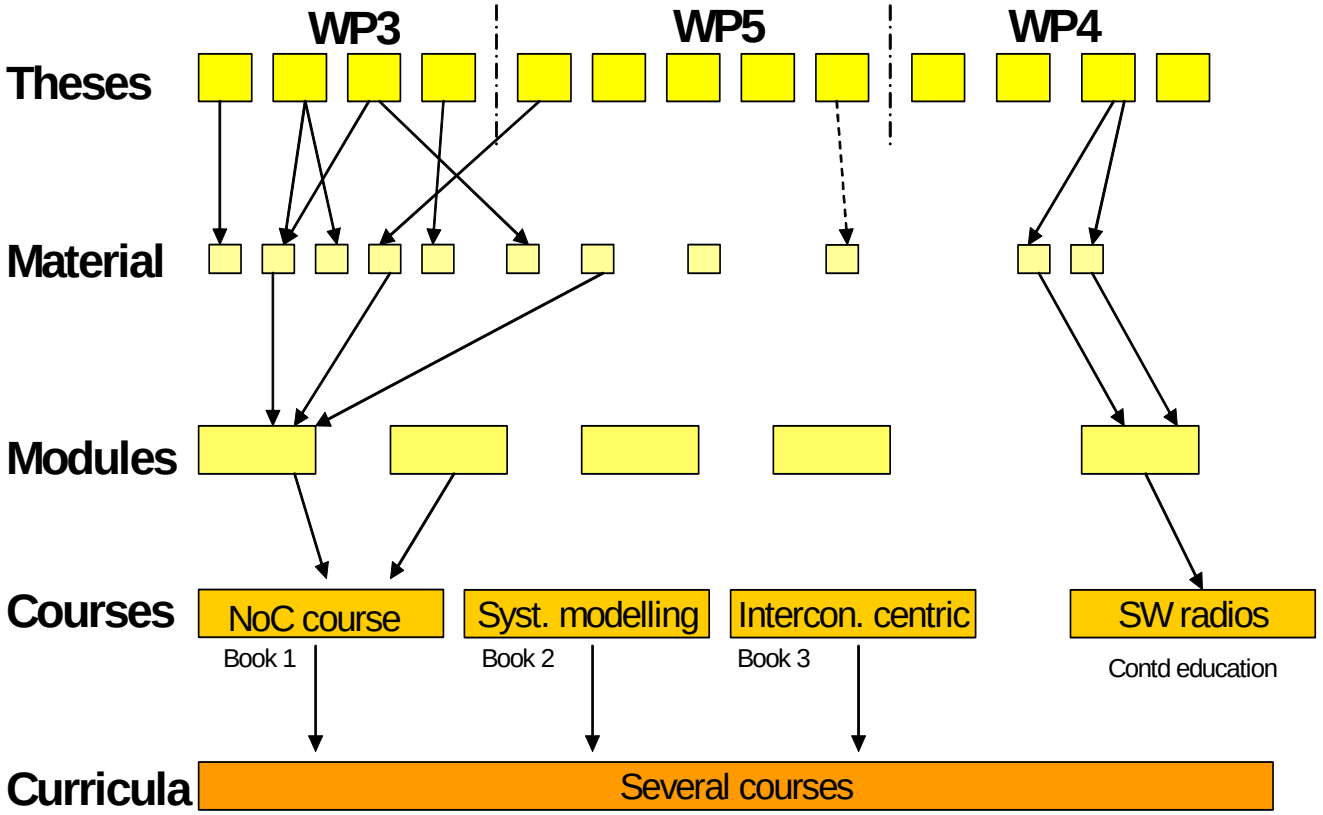
Time-to-education

- Faster and more global integration of research results to education
- Joint European efforst: SoC-Mobinet
- Joint Sino-Swedish effort: Training of of the traineers for 50 000 new IC/SOC designers in Asia
  - KTH-Zhejian Joint SoC Center 2004 in Hangzhou and in Kista
  - Expansion to Shanghai (Fudan) and Grenoble 2005
- Open invitation to new book serie on SoC education with focus on non-incremental curriculum improvement with new enabling technologies
  - Simultaneous publishing in Europa, USA, and China

Time-to-Education: Soc-Mobinet EU IST project



Time-to-Education: SoC Mobinet EU IST project



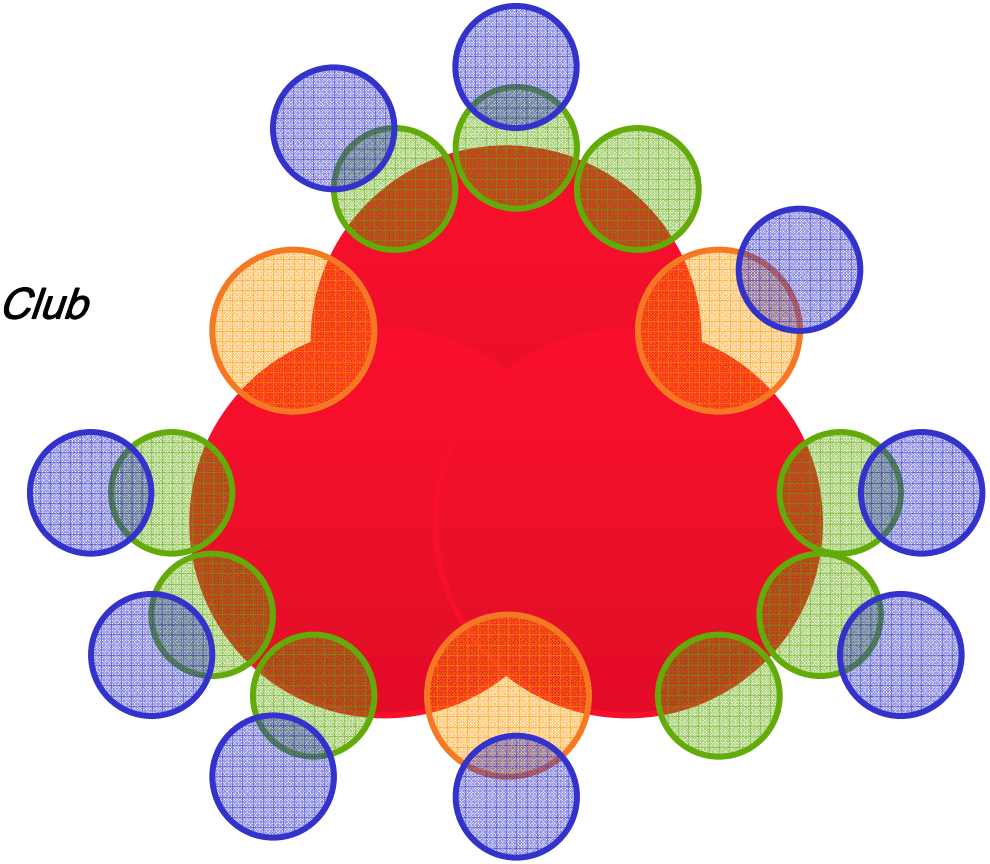
Book 1: Networks on Chip, Axel Jantsch et al, Kluwer
Book 2: System modelling and analysis, Axel Jantsch et al, Kaufmann
Book 3: Interconnect Centric Design, Jari Nurmi et al, Kluwer

Structure of the project

MSc

PhD

SoC-MOBI-*Club*



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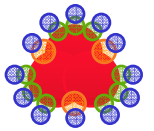
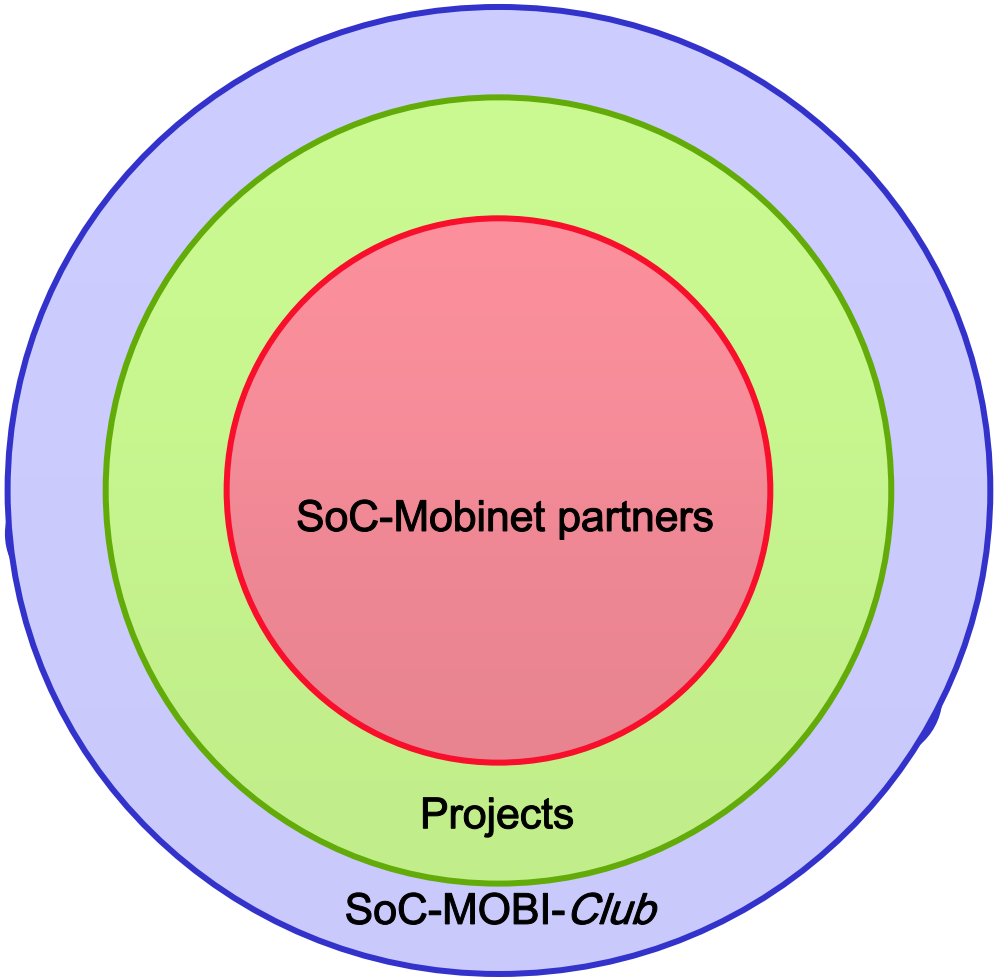
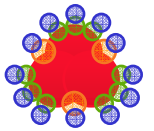




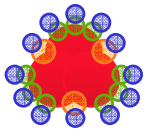
Major achievements



- Research
  - ***60*** Master thesis projects
  - ***10*** PhDs (3 finished)
  - ***8*** industrial projects
  - ***22*** SoC-Mobi-*Club* members
  - ***54*** research papers
  - ***21*** are *joint* SoC-Mobinet publications
  - ***16*** chapters in 3 new SoC books (2 edited by SoC-Mobinet)

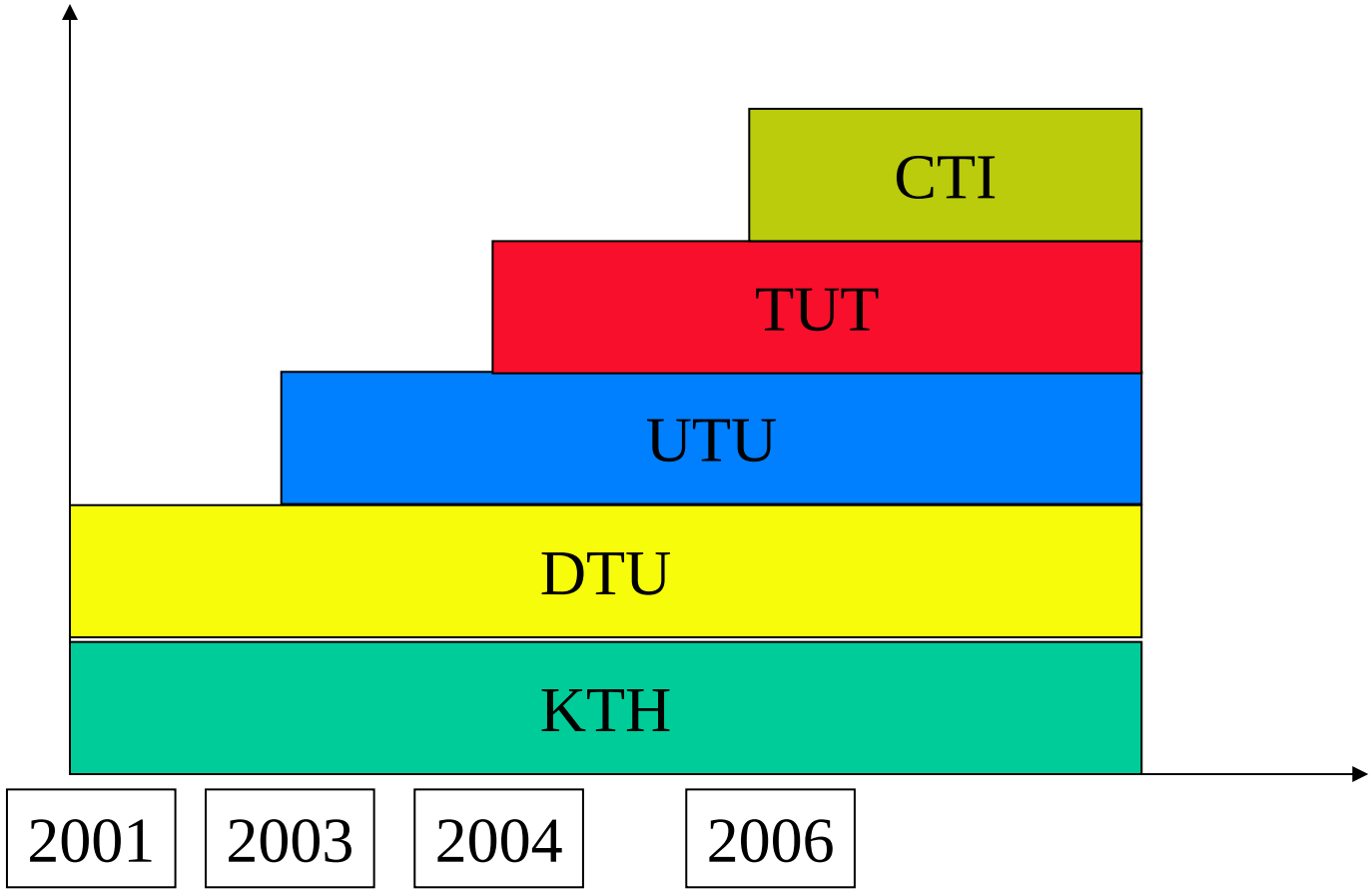
Partner	MSc	PhD	other
KTH	13	2	0
TUT	5	4	0
DTU	20	2	0
CTI	13	1	0
UTU	9	1	0
Acreo	0	0	2
Infineon	0	0	3
Spirea	0	0	3
Total	60	10	8

Major achievements



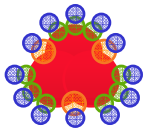
- Teaching
  - ***4*** new courses
    - Based on the gap analysis made in year 1
    - ***1*** new text book
    - 28.5 ECTS
  - ***5*** new course modules
    - 13.5 ECTS
  - ***42*** ECTS close to 1-year full programe
  - Courses are available through the SoC-Mobinet courseware website (www.imm.dtu.dk/SoC-Mobinet)
  - ***16+1*** training courses
    - 826 participants
    - 20 participants for Software Defined Radios
  - e-learning concept concieved, developed and tested with SoC-Mobinet

International Master Programme



Challenge: admission requirements, candidate selection

Education



		MSc 2001	MSc 2004	MSc 2007	PhD 2001	PhD 2004	PhD 2007
KTH	A strict SoC profile	0	60	60	2	4	4
	Reasonable SoC profile	10	10	30	5	20	30
TUT	A strict SoC profile	0	35	60	2	5	10
	Reasonable SoC profile	25	35	70	8	10	15
DTU	A strict SoC profile	6	13	10	1	3	5
	Reasonable SoC profile	5	9	15	2	3	5
CTI	A strict SoC profile	0	0	15	0	1	0
	Reasonable SoC profile	7	14	0	0	3	4
UTU	A strict SoC profile	4	7	15	0	1	3
	Reasonable SoC profile	5	6	10	0	2	3
Total		62	189	285	19	52	79

Continued Education

Course List

(D2:1 section 6)

Name	Location	Year	Part's
Workshop on SoC&SiP (Network on chip)	Villach	01	80
SoC Seminar	Tampere	01	146
Course on Enabling Technologies for Reconf. Computing	Tampere	01	35
Course on Amplifier Linearization & Dynamic Range Reduction	Norrköping	01	38
MATLAB WS w SoC-Mobinet relevant Topics	Villach	02	45
1:st Workshop on System C	Villach	02	45
Course on Digital System Engineering	Espoo	02	20
Workshop on Electrical Issues in SoC/SoP	Florence (ESSIRC)	02	52
Tutorial on Design & Verification of Embedded Computing Systems	Copenhagen (NorChip)	02	16

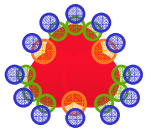
Continued Education

Course List (Cont'd)

(D2:1 section 6)

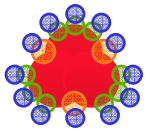
Name	Location	Year	Part's
Course on SOC Modelling Design & Validation	Tampere	02	67
SoC Seminar 2002	Tampere	02	168
2:nd Workshop on SoC & SystemC	Villach	02	45
Workshop on Processors for SoC integration	Villach	02	23
Course on Issues in Embedded processor Architecture Design for SoC	Tampere (Nokia)	03	25
Tutorial on Performance of On-Chip Communication Networks	Riga (NorChip)	03	7
Tutorial on Pondering the MOS-transistor in the 21:st Century	Riga (Norchip)	03	20
Tutorial on Re-configurable Computing	Tampere	03	72
Seminar on Software Defined Radio	Kista	04	20*

e-learning



- Conceived and developed at KTH
  - Template for e-learning
- Contents tested at KTH
- Distant learning based version at DTU
  - 2004: 25 students (17 passed)
  - Very good feedback from students
- Special version for continuing education
  - Focus on SME's
  - Open to all

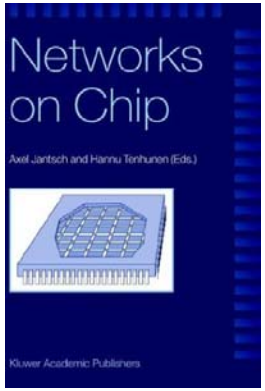
Courses



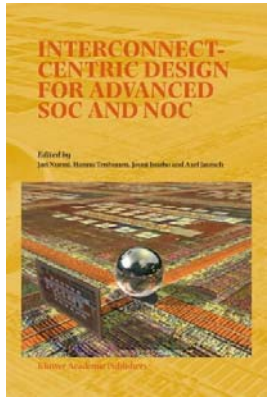
Course	Level	Material	ECTS
Network-on-Chip	Graduate	• Textbook: Kluwer book on Networks on Chip • Slides • Exercises • Lecturer instructions	6.0
System modelling	Graduate	• Textbook: Elsevier book on Modeling Embedded Systems and SoC's • Slides • Exercises • Lecturer instructions	7.5
Interconnect centric Design	Graduate	• Textbook: Kluwer book on "Interconnect-Centric Design for Next Generation SoC/NoC • Slides • Exersises • Lecturer instructions	5.0
Introduction to codesign	Undergraduate	• Lecture notes • Slides • Exersises • Lecturer instructions	10.0
Software defined radios	Continued training	• Slides	n/a

Courseware

System Modeling
[KTH]



Network-on-Chip
[KTH, TUT, UTU]



Interconnect-Centric Design
[KTH, TUT, UTU, DTU]

Multiprocessor System-on-Chip
[DTU]

Integration with China

- Transfering the educational program to double the number of SoC engineers in world
  - Joint Cino-Euro Center on Education and Research (SECER)
  - Close interaction with European industries (Infineon, Phillips, ST-Microelectronics, Nokia, Ericsson)
  - Formulated as joint EU Asia link proposal with agreements between key universities
- Providing the future leadership for CTO, R&D directors, and R&D managers of emerging companies and corporations
  - Educating Multi-Cultural Multi-National Future Leaders in Electronic Engineering

SECER objectives

- To develop its industry of software and integrated circuits (IC), the Chinese government decided in 2001 to train 40,000 IC designers and 10,000 supporting engineers by the year of 2010
- Based on the **existing partnership and expertise** in IC education and research at Zhejiang University, China (ZJU), Fudan University, Royal Institute of Technology, Sweden (KTH) and Institut National Polytechnique de Grenoble of France (INPG) agree to introduce into China a curriculum development system on SoC (System-on-Chip) at post-graduate level
- To establish a **Sino-Euro Centre of Education & Research (SECER)** in the field of SoC education, research and in-service training

SECER activities

- **➔Joint international Master's degree programmes**
  - SECRE will teach a joint international Master of Science (MSc) programme in SoC to students in ZJU, China at the initial stage. Based on its success in course development, students from all over the world, with specific focus on students from Asia and Australia will be enrolled at the next stage. All courses will be given in English. KTH, INPG and ZJU will jointly take the responsibility of quality management and quality control of the education.
- **➔Joint PhD degrees and/or exchange of PhD students**
  - A limited number of excellent students will be selected for PhD studies for joint degrees or as exchange PhD students. The host university or the advisor at the host university should arrange a scholarship for each visiting PhD students during his/her stay at the host university.
- **➔Joint research groups, joint research publications in the name of the Center, and exchange of researchers**

SECER tasks

- **The Centre will develop joint Master degree programs on SoC together with the new curriculum system and required mechanisms of teaching, assessment, and evaluation**. These programmes won't be a simple copy of any of the involved project universities but a hybrid of excellence of them.
- **Master thesis projects** will also be arranged by KTH and INPG. It will be an international course. And, will familiarize students with European education system while studying in China and pave their way for further study in Europe.
- **It will adopt ECTS system** to quantify students' workload and their learning outcomes so that students can bring their credits to partner universities for further study.
- **Research integration:** It will help to **set up a close professor-to-professor relationship among professors through the joint endeavour of teaching this international course**.
- Being fully established, the Joint Centre will get its international programme accredited by **European accreditation** organizations from Europe so that it can provide students with a European accredited degree at the conclusion of the project (2007)
- Enrol **international students from other countries in Asia and Australia** along with exchange students from Europe

Technical leadership in SoC

- European electronics industry, particularly north Europe, is **outsourcing** their manufacturing to China/Asia. In China, the situation is complementary. They have recently started to establish their system R & D centre in north Europe**.**
- The process of **globalisation urgently demands qualified engineers and future leaders with international background**
- **Emphasis on leadership in electronic engineering** will be developed and implemented at master and Ph.D. levels.
- In order to **breed a new generation of leaders for future high-technique companies in electronics, we aim to develop a multi-national multi-cultural educational platform through Europe-China collaboration in this program**.
- **We aim to educate future leaders for those small start-up and median-size enterprises (SME) and enhance their competence in global competition**.
- **Need to be trained in multiple cultural environments**.

Technical leadership in SoC: Instruments

- The action will set up a **sandwich program between Europe and China**. Students from both China and from Europe will take courses and do thesis works in guest universities. We encourage that each student will stay at least three countries during the course of his/her study so that they are highly exposed to different culture environment.
- The target student groups are those who **will pursue master degree and Ph.D. degree**. These students will join either industry in China or in Europe, or they remain in universities and academia, as future teachers. The program also involves guest teachers.
- The activities of **joint supervision of master thesis works and joint Ph.D. education in the project**
- For leadership training, students will be arranged to have **1-3 months internship in industry in these involved countries**.