SoC 2009
International Symposium on System-on-Chip

Tampere Hall, Yliopistonkatu 55

Tampere, Finland, Oct. 6-7, 2009

The 11th Annual SoC Event in Tampere

Organized by Department of Computer Systems, Tampere University of Technology.

Technical co-sponsorship by IEEE Circuits and Systems Society.

Financial sponsors: ST-Ericsson, Nokia, and IEEE Finland Section.

TAMPERE UNIVERSITY OF TECHNOLOGY

IEEE

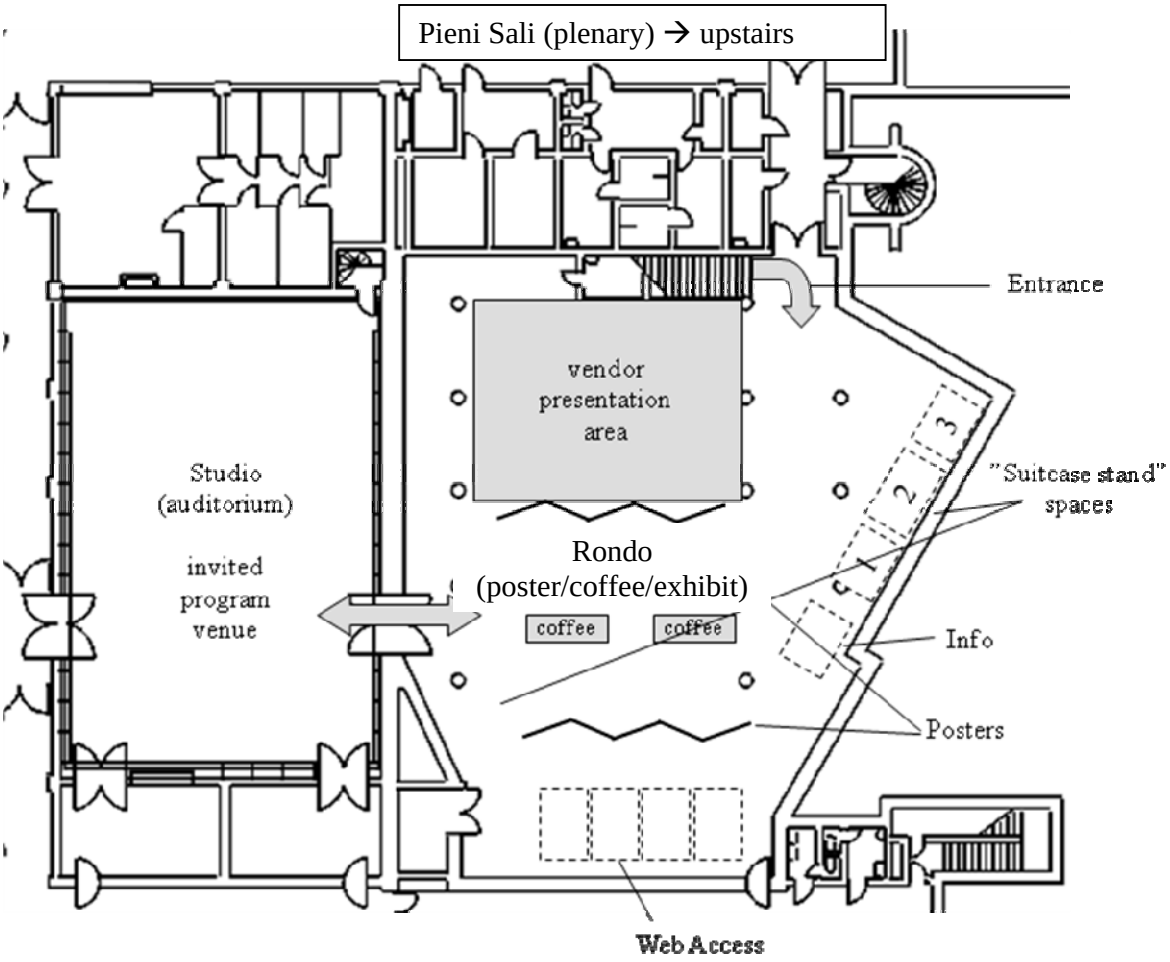
Venue

Tampere Hall was inaugurated in 1990 and is the largest congress and concert centre in Scandinavia. Its modern architecture and integral works of art make Tampere Hall a sight worth seeing in itself. Tampere Hall is located on the edge of Sorsapuisto Park, beside Sorsalampi duck pond, within a short walking distance of the city centre.

Tampere – the SoC city – is situated in the heart of beautiful Finnish Lakeland. The banks of the Tammerkoski rapids still feature old traditional industrial buildings which have now been converted to house pleasant restaurants, pubs or high-tech companies. Tampere is also a city of theatres, arts, sciences, sport and modern industrial culture.

Exhibition

There is an exhibit of SoC technology and tool vendors, and an associated industry program track interleaved with the invited and contributed program.



List of exhibitors

- Synopsys
- EBSCO
- Springer

INTERNATIONAL SYMPOSIUM ON SYSTEM-ON-CHIP 2009

Tampere Hall, Tampere, Finland, October 6-7, 2009

PROGRAMME AT A GLANCE

MONDAY Oct. 5
09:00 - 17:00 Tutorial on Signal Processing in Wireless Systems
17:00 – 17:30 Reception and early registration (Tampere Hall)
17:15 – 19:00 IEEE Finland Section meeting

TUESDAY Oct. 6
09:00 – 10:00 Registration and Coffee
10:00 – 10:15 Opening
10:15 – 11:00 DYNAMICALLY RECONFIGURABLE SYSTEM DESIGN (Koen Bertels, TU Delft)
11:00 – 12:00 Poster1 || Industry1 Coffee
12:00 – 13:15 Lunch
13:15 – 14:00 3-D INTEGRATION FROM SYSTEM DESIGN PERSPECTIVE (Dragomir Milojevic, ULB/IMEC)
14:00 – 15:00 SESSIONS: Analysis and Estimation Methods || Network-on-Chip and Inter-Chip Communications
15:00 – 16:00 Poster2 Coffee
16:00 – 16:45 SCALABLE REAL-TIME COMPUTING ON TRANSPARENTLY OPERATED MANY-CORE PLATFORMS (Tapani Ahonen, TUT)
16:45 – 18:00 Panel discussion: Real-time embedded signal processing implementation – how?

18:00 – 19:00 Reception in exhibit hall

WEDNESDAY Oct. 7
09:00 – 09:15 SiPS 2009 opening
09:15 – 10:00 CHALLENGES OF SIGNAL PROCESSING IMPEMENTATIONS ON MOBILE DEVICES (Henry Tirri, Nokia) – plenary with SiPS 2009
10:00 – 11:00 Industry2 Coffee
11:00 – 12:20 SESSION: Advanced Platform Architectures
12:20 – 13:20 Lunch
13:20 – 14:40 SESSION: Application-Specific Processors and Architectures
14:40 – 15:40 Exhibit break (SiPS posters) Coffee
15:40 – 16:40 SESSION: System-Level Design Methodology
16:40 – 17:00 Short break
17:00 – 17:45 BEING GLOBALLY ENERGY-AWARE IN DSP SYSTEM DESIGN (Chong-Min Kyung, KAIST) – plenary with SiPS 2009
17:45 – 18:00 Closing SoC 2009 and SiPS 2010 preview

19:00 – 22:00 Banquet (Viking Restaurant Harald) – plenary with SiPS 2009

SoC 2009 Detailed Program Schedule

TUESDAY Oct.6

Welcome coffee

SESSION: Opening
Location: Studio

10:00 WELCOME TO SOC 2009
Jari Nurmi, *Tampere University of Technology, Finland*

SESSION: Keynote
Location: Studio
Chair: Jari Nurmi, TUT

10:15 DYNAMICALLY RECONFIGURABLE SYSTEM DESIGN
Koen Bertels, *TU Delft, The Netherlands*

SESSION: Industry1 and coffee
Location: Rondo

11:00 **FPGA: The Verification Platform of the Future?**
Antti Innamaa, *Synopsys, Finland*

SESSION: Poster 1 and coffee
Time: 11:00 – 12:00
Location: Rondo

Simultaneous PVT-Tolerant Voltage-Island Formation and Core Placement for Thousand-Core Platforms
Sohaib Majzoub, Resve Saleh, Steve Wilton, Rabab Ward
Department of Electrical and Computer Engineering, University of British Columbia, Canada

Fault-Tolerant Communication over Micronmesh NOC with Micron Message-Passing Protocol
Heikki Kariniemi and Jari Nurmi
Department of Computer Systems, Tampere University of Technology, Finland

Adaptive Circuit Block Model for Power Supply Noise Analysis of Low Power System-on-Chip
Matthias Eireiner[1], Paul Wallner[2], Andreas Schoene[2], Stephan Henzler[2], Ulrich Fiedler[2], Doris Schmitt-Landsiedel[1]
[1]Technical University Munich, Germany [2]Infineon Technologies AG, Munich, Germany

Parameterizing Simulated Annealing for Distributing Kahn Process Networks on Multiprocessor SoCs
Heikki Orsila, Erno Salminen, Timo D. Hämäläinen
Tampere University of Technology, Finland

Energy and Bandwidth Aware Mapping of IPs onto Regular NoC Architectures Using Multi-Objective Genetic Algorithms
KSHITIJ BHARDWAJ[1] and RABINDRA JENA[2]
[1]Institute of Engg. & Tech, DAVV, India [2]Institute of Management & Tech., India

Physical realization oriented area-power-delay tradeoff exploration
Volker Gierenz[1], Christian Panis[1], Jari Nurmi[2]
[1]Catena Radio Design bv,, The Netherlands [2]Tampere University of Technology, Finland

Testing and Diagnosis of Faults in Template-Based Asynchronous Circuits
Behnam Ghavami[1], Hamid_Reza Zarandi[1], Arezoo Salarpour[2], Hossein Pedram[1]
[1]Amirkabir University of Technology, Iran [2]University of Science and Technology, Iran

Dynamic Workload Peak Detection For Slack Management
Aleksandar Milutinovic[1], Kees Goossens[2], Gerard J.M. Smit[1]
[1]University of Twente, The Netherlands [2]NXP, The Netherlands

Building Asynchronous Routers with Independent Sub-Channels
Wei Song and Doug Edwards
University of Manchester, UK

SESSION: Lunch
Location: Restaurant Fuuga

12:00 – 13:15

SESSION: Invited 2
Location: Studio
Chair: Jari Nurmi, TUT

13:15 3-D INTEGRATION FROM SYSTEM DESIGN PERSPECTIVE
Dragomir Milojevic, *Université Libre de Bruxelles / IMEC, Belgium*

SESSION: Analysis and Estimation Methods
Location: Studio
Chair: Olli Vainio, TUT

14:00 Soft NMR: Exploiting Statistics for Energy-Efficiency
Eric Kim, Rami Abdallah, Naresh Shanbhag
University of Illinois at Urbana Champaign, USA

14:20 Performance Analysis of LTE Protocol Processing on an ARM based Mobile Platform
David Szczesny[1], Anas Showk[1], Sebastian Hessel[1], Uwe Hildebrand[2], Valerio Frascolla[2], Attila Bilgic[1]
[1]Institute for Integrated Systems, Ruhr-Universität Bochum, D-44780 Bochum, Germany, [2]Comneon GmbH, D-90449 Nürnberg, Germany

14:40 Performance Modeling of Parallel Applications on MPSoCs
Marco Lattuada, Christian Pilato, Antonino Tumeo, Fabrizio Ferrandi
Politecnico di Milano, Italy

SESSION: Network-on-Chip and Inter-Chip Communications
Location: Rondo
Chair: Heikki Kariniemi, TUT

14:00 Impact of Device Variability in the Communication Structures for Future Synchronous SoC Designs
Faiz ul Hassan, Binjie Cheng, Wim Vanderbauwhede, Fernando Rodriguez
University of Glasgow, UK

14:20 Flexible DOR Routing for Virtualization of Multicore Chips
Frank Olaf Sem-Jacobsen[1], Tor Skeie[1], Samuel Rodrigo[2], José Flich[2], Davide Bertozzi[3], Simone Medardoni[3]
[1]Networks and Distributed Systems, Simula Research Laboratory, Lysaker, Norway, [2]Parallel Architectures Group, Technical University of Valencia, Valencia, Spain, [3]ENDIF, Department of Engineering, University of Ferrara, Ferrara, Italy

14:40 Automatic Generation of Memory Interfaces
David Kammler[1], Bastian Bauwens[1], Ernst Martin Witte[1], Gerd Ascheid[1], Rainer Leupers[1], Heinrich Meyr[1], Anupam Chattopadhyay[2]
[1]ISS, RWTH Aachen University, [2]CoWare India Private Ltd

SESSION: Poster 2 and coffee
Time: 15:00 – 16:00
Location: Rondo

Two Phase Clocked Adiabatic Static CMOS Logic
Nazrul Anuar Nayan[1], Yasuhiro Takahashi[2], Toshikazu Sekine[2]
[1]Graduate School of Engineering, Gifu University, Japan [2]Gifu University, Japan

Evaluation of Static and Dynamic Task Mapping Algorithms in NoC-Based MPSoCs
Ewerson Carvalho, César Marcon, Ney Calazans, Fernando Moraes
PUCRS, Brazil

Minimizing area costs in GPS applications on a programmable DSP by code compression
Piia Saastamoinen[1], Jari Nurmi[1], Ilkka Saastamoinen[2], Mikko Laiho[2]
[1]Tampere University of Technology, Department of Computer Systems, [2]Atheros Communications, Tampere, Finland

Scheduling Framework for Real-time Dependable NoC-Based Systems
Mihkel Tagel, Peeter Ellervee, Gert Jervan
Tallinn University of Technology, Estonia

Yield-oriented Evaluation Methodology of Networks-on-Chip Routing Implementations
Samuel Rodrigo[1], Carles Hernández[1], José Flich[1], Federico Silla[1], José Duato[1], Simone Merdardoni[2], Davide Bertozzi[2], Andres Mejia[3], Donglai Dai[3]
[1]UPV, Spain [2]UNIFE, Italy [3]INTEL, USA

A Multi-Core Signal Processor for Heterogeneous Reconfigurable Computing
Davide Rossi[1], Fabio Campi[2], Antonio Deledda[1], Claudio Mucci[2], Stefano Pucillo[2], Sean Whitty[4], Rolf Ernst[4], Stephane Chevobbe[5], Stephane Guyetant[5], Matthias Kühnle[6], Michael Hübner[6], Jürgen Becker[6], Wolfram

Putzke-Roeming[7] *[1]ARCES,University of Bologna, Italy, [2]ST Microelectronics, Agrate Brianza, Italy, [4]Technische Universität Braunschweig, Germany, [5]CEA, Paris, France, [6]ITIV, University Of Karlsruhe, Germany, [7]Thomson, Germany*

RTL-to-Layout Implementation of an Embedded Coarse Grained Architecture for Dynamically Reconfigurable Computing in Systems-on-Chip
Fabio Campi[1], Ralf König[2], Michael Dreschmann[2], Moritz Neukirchner[3], Damien Picard[4], Michael Jüttner[5], Eberhard Schüler[6], Antonio Deledda[7], Davide Rossi[7], Alberto Pasini[1], Michael Hübner[2], Jürgen Becker[2], Roberto Guerrieri[7]
[1]STMicroelectronics, Italy [2]ITIV, University of Karlsruhe, Germany [3]Technical University of Braunschweig, Germany [4]Université de Bretagne Occidentale, France [5]Technical University of Chemnitz, Germany, [6]PACT XPP Technologies, Germany [7]ARCES, University of Bologna, Italy

Analysis of Memory Access Optimization for Motion Compensation Frames in MPEG-4.
Haitham Habli[1], Johan Ersfolk[2], Johan Lilius[1]
[1]Åbo Akademi university, Finland [2]TUCS and Åbo Akademi university, Finland

Pathfinding: A design methodology for fast exploration and optimization of 3D-stacked integrated circuits
Dragomir Milojevic[1], Riko Radojcic[2], Roger Carpenter[3], Pol Marchal[4]
[1]ULB, Belgium [2]Qualcomm, USA [3]Javelin DA, USA [4]IMEC, Belgium

SESSION: Invited 3
Location: Studio
Chair: Jari Nurmi, TUT

16:00 SCALABLE REAL-TIME COMPUTING ON TRANSPARENTLY OPERATED MANY-CORE PLATFORMS
Tapani Ahonen, *TUT, Finland*

SESSION: Panel Discussion: Real-time embedded signal processing implementation – how?
Time: 16:45 – 18:00
Location: Studio

SESSION: Reception in the exhibit
Time: 18:00 - 19:00
Location: Rondo

WEDNESDAY Oct. 7

SESSION: Opening of SiPS 2009
Location: Pieni Sali
Chair: Jari Nurmi, TUT

SESSION: Invited 4 – plenary with SiPS 2009
Location: Pieni Sali
Chair: Markku Renfors, TUT

09:15 SIGNAL PROCESSING IMPLEMENTATION CHALLENGES IN MOBILE TERMINALS
Henry Tirri, *Nokia, USA*

SESSION: Industry 2 and coffee
Location: Rondo

10:00 t.b.d
Petri Solanti, *Synopsys Finland Oy, Finland*

SESSION: Advanced Platform Architectures
Location: Studio
Chair: Tapani Ahonen, TUT

11:00 Multi-Compartment: A New Architecture for Secure Co-Hosting on SoC
Joël Porquet[1], Christian Schwarz[1], Alain Greiner[2]
[1]STMicroelectronics, France [2]UPMC/LIP6, France

11:20 Performance Analysis of Multi-Channel Memories in Mobile Devices
Jari Nikara, Eero Aho, Petri Tuominen, Kimmo Kuusilinna
Nokia Research Center, Finland

11:40 System Architecture for 3GPP LTE Modem using a Programmable Baseband Processor

Di Wu, Johan Eilert, Dake Liu, Anders Nilsson, Eric Tell, Erik Alfredsson
Linköping University, Sweden

12:00 On the Performance of 3GPP LTE Modem using a Programmable Baseband Processor
Zhenyu Tu, Meng Yu, Daniel Iancu, Mayan Moudgill, John Glossner
Sandbridge Technologies Inc, USA

SESSION: Lunch
Location: Restaurant Fuuga

12:20 – 13:20

SESSION: Application-Specific Processors and Architectures
Location: Studio
Chair: Erno Salminen, TUT

13:20 Instruction Merging to Increase Parallelism in VLIW Architectures
Guillermo Payá-Vayá, Javier Martín-Langerwerf, Florian Giesemann, Holger Blume, Peter Pirsch
Institute of Microelectronic Systems, Leibniz Universität Hannover , Germany

13:40 Efficient Software Cache for H.264 Motion Compensation
Arnaldo Azevedo and Ben Juurlink
Delft University of Technology, The Netherlands

14:00 A DSP architecture optimized for wireless baseband
Chris Rowen, Peter Nuth, Stuart Fiske, Marcus Binning, Sam Khouri
Tensilica, inc., USA

14:20 Mapping of the FFT on a Reconfigurable Architecture targeted to SDR Applications
Fabio Garzia[1], Roberto Airoldi[1], Carmelo Giliberto[2], Claudio Brunelli[2], Jari Nurmi[1]
[1]TUT, Finland [2]NOKIA, Finland

SESSION: Exhibit break, SiPS posters and coffee
Location: Rondo

14:40 – 15:40

SESSION: System-Level Design Methodology
Location: Studio
Chair: Tapani Ahonen, TUT

15:40 A Checkpoint/Restore Framework for SystemC-Based Virtual Platforms
Stefan Kraemer[1], Rainer Leupers[1], Dietmar Petras[2], Thomas Philipp[2]
[1]RWTH-Aachen University, Germany [2]CoWare, Germany

16:00 Automated Instrumentation of FPGA-based Systems for System-level Transaction Monitoring
Paul McKechnie[1], Michaela Blott[2], Wim Vanderbauwhede[3]
[1]Institute for System Level Integration, UK [2]Xilinx, Ireland [3]University of Glasgow, UK

16:20 Characterising Embedded Applications using a UML Profile
Sanna Määttä[1], Leandro Soares Indrusiak[2], Luciano Ost[3], Leandro Möller[4], Manfred Glesner[4], Fernando Gehm Moraes[3], Jari Nurmi[1]
[1]Tampere University of Technology, Finland [2]University of York, UK [3]Catholic University of Rio Grande do Sul, Brazil [4]Technische Universität Darmstadt, Germany

SESSION: Short break
Location: Rondo

16:40 – 17:00

SESSION: Invited 5 – plenary with SiPS 2009
Location: Pieni Sali
Chair: Wonyong Sung, Seoul National University

17:00 BEING GLOBALLY ENERGY-AWARE IN DSP SYSTEM DESIGN
Chong-Min Kyung, *KAIST, Korea*

SESSION: Closing of SoC 2009 and preview of SiPS 2010
Time: 17:45 – 18:00
Location: Pieni Sali

SESSION: Banquet
Time: 19:00 - 22:00
Location: Viking Restaurant Harald

SoC 2009 Tampere Hall October 6-7, 2009

General Chair's message

Welcome to Tampere – The SoC City!

This is the 11th annual SoC event organized in Tampere, following the tradition of the previous years by providing a high-level invited lecture program, scientific paper program, a small exhibit, industrial program track, panel discussion, appealing social events – and reasonable amounts of coffee (as again pointed out in this program leaflet). In the scientific program we have selected 17 oral presentations and 18 posters from the quality paper submissions. This year we are co-located with IEEE Workshop on Signal Processing Systems on October 7-9. This is shown in plenary invited and poster/coffee sessions and a joint banquet between the events. The participants of SoC and SiPS represent over 20 different nationalities.

This year we can also enjoy of a high-calibre tutorial on Signal processing in wireless communication systems, delivered by professors Markku Renfors (TUT), Markku Juntti (University of Oulu, Finland), Joseph Cavallaro (Rice University, USA), and Mikko Valkama (TUT).

The International Symposium on System-on-Chip has become The Place for the industry and academics in the SoC field to meet each others in a casual atmosphere. I hope that the presentations and all the informal discussions during the breaks and in the social events will inspire each of you in doing research and development towards more successful Systems-on-Chip.

Thanks to the numerous people who have contributed to the success of this event.

Next year the SoC symposium will take place on October 6-7 with a tutorial on October 5. The location will be exactly the same, mark your calendars and keep watching the details at **http://soc.cs.tut.fi/**

See you in Tampere also next year!

Prof. Jari Nurmi
General Chairman
SoC 2009