SoC 2010
International Symposium on System-on-Chip

Tampere Hall, Yliopistonkatu 55

Tampere, Finland, Sept. 29-30, 2010

The 12th Annual SoC Event in Tampere

Organized by Department of Computer Systems, Tampere University of Technology.

Technical co-sponsorship by IEEE Circuits and Systems Society.

Financial sponsors: ST-Ericsson, Nokia, Recore Systems, Mentor Graphics, and IEEE Finland Section.

TAMPERE UNIVERSITY OF TECHNOLOGY

IEEE

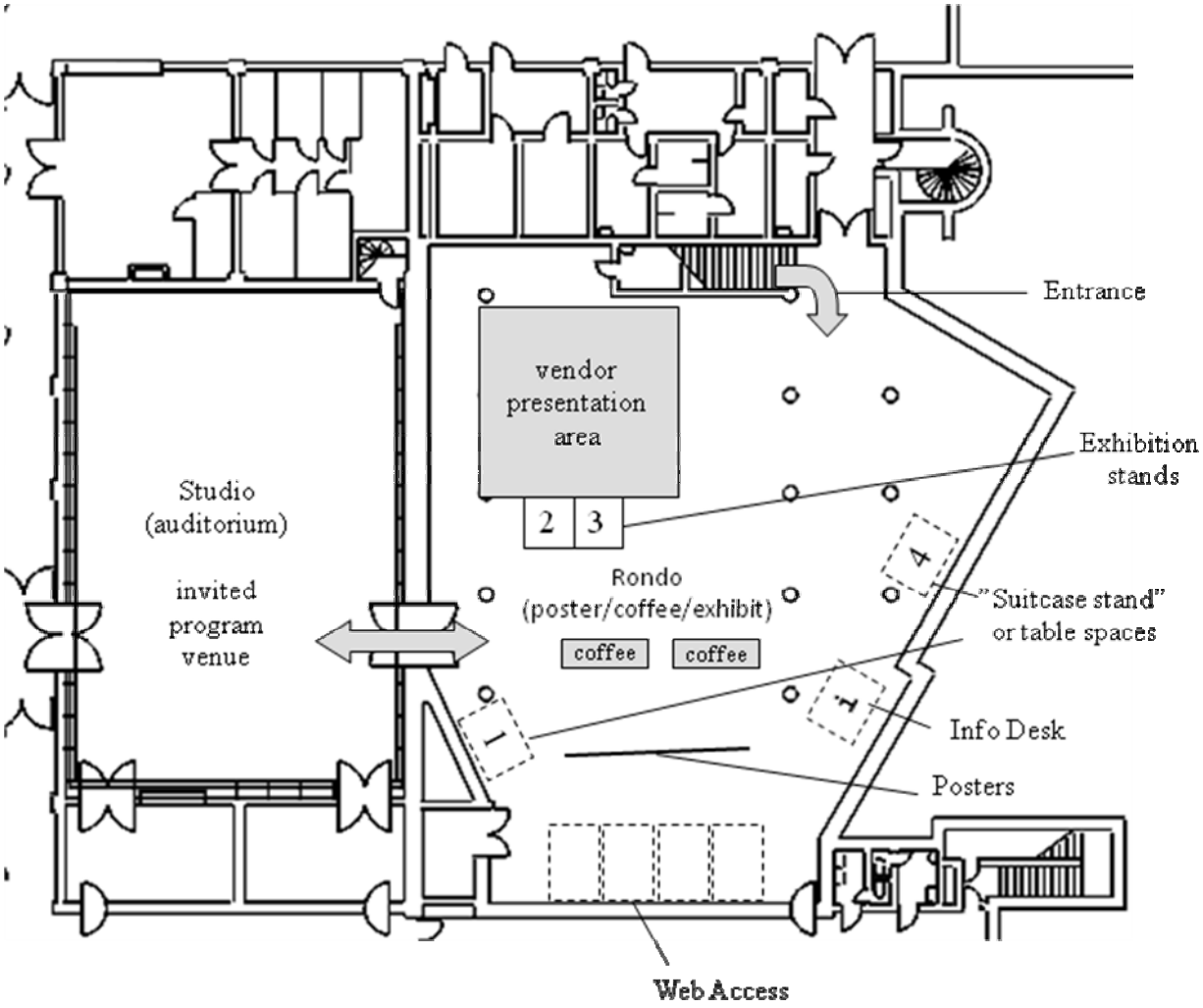
Venue

Tampere Hall was inaugurated in 1990 and is the largest congress and concert centre in Scandinavia. Its modern architecture and integral works of art make Tampere Hall a sight worth seeing in itself. Tampere Hall is located on the edge of Sorsapuisto Park, beside Sorsalampi duck pond, within a short walking distance of the city centre.

Tampere – the SoC city – is situated in the heart of beautiful Finnish Lakeland. The banks of the Tammerkoski rapids still feature old traditional industrial buildings which have now been converted to house pleasant restaurants, pubs or high-tech companies. Tampere is also a city of theatres, arts, sciences, sport and modern industrial culture.

Exhibition

There is an exhibit of SoC technology and tool vendors, and an associated industry program track interleaved with the invited and contributed program.



List of exhibitors

- CRISP Project
- Freescale Semiconductor
- IEEE GOLD and Student Activities
- Mentor Graphics

INTERNATIONAL SYMPOSIUM ON SYSTEM-ON-CHIP 2010

Tampere Hall, Tampere, Finland, September 29-30, 2010

PROGRAMME AT A GLANCE

TUESDAY Sept. 28

09:00 - 17:00 Tutorial on Dependable Hardware and Software for Embedded Multicore Computing Platforms

17:00 – 18:00 Reception and early registration (Tampere Hall)

WEDNESDAY Sept. 29

09:00 – 10:00 Registration and Coffee
10:00 – 10:15 Opening
10:15 – 11:00 PRESENT AND FUTURE CHALLENGES IN DEVELOPING A MANYCORE RTOS (Eric Verhulst, Altreonic)
11:00 – 12:00 Poster1 || Industry1 Coffee
12:00 – 12:45 RECONFIGURABLE EMBEDDED MULTICORE PROCESSOR FOR STREAMING APPLICATIONS (Paul Heysters, Recore Systems)
12:45 – 14:00 Lunch
14:00 – 15:00 SESSIONS: SoC Applications || Network-on-Chip
15:00 – 16:00 Poster2 Coffee
16:00 – 16:45 INTRODUCING NEW FEATURES FOR THE ARM ARCHITECTURE (David Brash, ARM)
16:45 – 18:00 Panel discussion: All Roads Lead to Manycore – or Do They?

19:00 – 22:00 Banquet (Restaurant Laterna)

THURSDAY Sept. 30

09:00 – 09:45 PORTABILITY OF SOFTWARE DEFINED RADIO IMPLEMENTATION (Heikki Berg, Nokia)
09:45 – 10:45 Poster 3 || Industry2 Coffee
10:45 – 11:25 SESSION: Testing and Dependability
11:25 – 12:25 SESSIONS: Design Methodology || Sensor Networks and Neural Networks
12:25 – 13:30 Lunch
13:30 – 14:15 MULTIPROCESSOR SYSTEM AND SOFTWARE DESIGN FOR DISTRIBUTED CONTROL APPLICATIONS (Samarjit Chakraborty, TU Munich)
14:15 – 15:15 Poster 4 Coffee
15:15 – 16:15 SESSION: Architecture Analysis and Optimization
16:15 – 17:00 PHYSICAL DESIGN ISSUES IN MP-SOC (Fabio Campi, STMicroelectronics)
17:00 – 17:20 Closing

18:00 – 21:00 Ice-hockey Tappara vs. TPS, Hakametsä Ice Hall

21:00 – 23:00 Farewell Supper, Brewery Restaurant Plevna

SoC 2010 Detailed Program Schedule

WEDNESDAY Sept. 29

Welcome coffee

SESSION: Opening
Location: Studio

10:00 WELCOME TO SOC 2010
Jari Nurmi, *Tampere University of Technology, Finland*

SESSION: Keynote
Location: Studio
Chair: Jari Nurmi, TUT

10:15 PRESENT AND FUTURE CHALLENGES IN DEVELOPING A MANYCORE RTOS
Eric Verhulst, *Altreonic, Belgium*

SESSION: Industry1 and coffee
Location: Rondo

11:00 Addressing Multi-core Design Challenges With Scalable TLM Modeling
Yossi Veller and Rami Rachamim, Mentor Graphics, USA

SESSION: Poster 1 and coffee
Time: 11:00 – 12:00
Location: Rondo

Hamming Distance Based 2-D Reordering With Power Efficient Don't Care Bit Filling: Optimizing the Test Data Compression Method
Usha Mehta[1], Kankar Dasgupta[2], Niranjan Devashrayee[1]
1) Nirma University, Ahmedabad, India, 2) SAC, ISRO, Ahmedabad, India

Energy-Aware Run-Time Mapping for Homogeneous NoC
Sun Guang, Li Yong, Zhang Yuanyuan, Su Li, Jin Depeng, Zeng Lieguang
Tsinghua University, China

Power Consumption Analysis and Energy Efficient Optimization for Turbo Decoder Implementation
Pallavi Reddy[1], Rasheed Al Khayat[2], Amer Baghdadi[2], Fabien Clermidy[1], Michel Jezequel[2]
1) CEA Grenoble, France 2) Telecom Bretagne, France

From Y-Chart to Seamless integration of Application Design and Performance Simulation
Subayal Khan[1], Eila Ovaska[1], Kari Tiensyrjä[1], Jari Nurmi[2]
1) VTT Technical Research Centre of Finland, 2)Tampere University of Technology, Finland

SESSION: Invited 2
Location: Studio
Chair: Jari Nurmi, TUT

12:00 RECONFIGURABLE EMBEDDED MULTICORE PROCESSOR FOR STREAMING APPLICATIONS
Paul Heysters, *Recore Systems, The Netherlands*

SESSION: Lunch
Location: Restaurant Fuuga

12:45 – 14:00

SESSION: SoC Applications
Location: Studio
Chair: Olli Vainio, TUT

14:00 Homogeneous MPSoC as Baseband Signal Processing Engine for OFDM Systems
Roberto Airoldi, Fabio Garzia, Omer Anjum, Jari Nurmi
Tampere University of Technology, Finland

14:20 Efficient Floating-Point Texture Decompression
Tomi Aarnio[1], Claudio Brunelli[1] Timo Viitanen[2]
1) Nokia Research Center, Finland, 2) Tampere University of Technology, Finland

14:40 A Flexible Integrated Cryptoprocessor for Authentication Protocols based on Hyperelliptic Curve Cryptography
Alexander Klimm
KIT-ITIV, Germany

SESSION: Network-on-Chip
Location: Rondo
Chair: Heikki Kariniemi, TUT

14:00 Process Variation and Layout Mismatch Tolerant Design of Source Synchronous Links for GALS Networks-on-Chip
Alessandro Strano[1], *Carles Hernàndez*[2], *Federico Silla*[2], *Davide Bertozzi*[1]
1)University of Ferrara, Italy, 2)Universidad de Valencia, Spain

14:20 Skip-links: A Dynamically Reconfiguring Topology for Energy Efficient NoCs
Chris Jackson and Simon J. Hollis
Department of Computer Science, University of Bristol, UK

14:40 Efficient Compensation of Delay Variations in High-Speed Network-on-Chip Data Links
Sebastian Höppner, Dennis Walter, Holger Eisenreich, René Schüffny
TU Dresden, Germany

SESSION: Poster 2 and coffee
Time: 15:00 – 16:00
Location: Rondo

Implementation and Benchmarking of FFT Algorithms on Multicore Platforms
Claudio Brunelli[1], *Roberto Airoldi*[2], *Jari Nurmi*[2]
1) Nokia Corporation, Finland, 2)Tampere University of Technology, Finland

Parameterized Decompression HW for a Program Memory Compression System
Piia Saastamoinen and Jari Nurmi
Tampere University of Technology, Finland

A Case Study of Hierarchically Heterogeneous Application Modelling Using UML and Ptolemy II
Sanna Määttä[1], *Leandro Soares Indrusiak*[2], *Luciano Ost*[3], *Leanrdo Möller*[4], *Manfred Glesner*[4], *Fernando Gehm Moraes*[3], *Jari Nurmi*[1]
1)Tampere University of Technology, Finland, 2)University of York, UK, 3)Catholic University of Rio Grande do Sul, Brazil, 4)Technische Universität Darmstadt, Germany

State Chart Refinement Validation from Approximately Timed to Cycle Callable Models
Rainer Findenig[1] *and Wolfgang Ecker*[2]
)1Upper Austrian University of Applied Sciences, Hagenberg, Austria, 2) Infineon Technologies AG, Germany

SESSION: Invited 3
Location: Studio
Chair: Jari Nurmi, TUT

16:00 INTRODUCING NEW FEATURES FOR THE ARM ARCHITECTURE
David Brash, *ARM, UK*

SESSION: Panel Discussion: All Roads Lead to Manycore – or Do They?
Time: 16:45 – 18:00
Location: Studio

SESSION: Banquet
Time: 19:00 - 22:00
Location: Restaurant Laterna, Puutarhakatu 11, Tampere

THURSDAY Sept. 30

SESSION: Invited 4
Location: Studio
Chair: Jari Nurmi, TUT

09:00 PORTABILITY OF SOFTWARE DEFINED RADIO IMPLEMENTATION
Heikki Berg, *Nokia, Finland*

SESSION: Industry 2 and coffee
Location: Rondo

09:45 High Quality HW from Efficient Algorithm Model
Petri Solanti, *Synopsys Finland Oy, Finland*

SESSION: Poster 3 and coffee
Time: 09:45 – 10:45
Location: Rondo

MCDA-Based Methodology for Efficient 3D-Design Space Exploration And Decision
Nguyen Anh Vu Doan[1], Frédéric Robert[2], Yves De Smet[3], Dragomir Milojevic[2]
1) BEAMS/CoDE-SMG - Université Libre de Bruxelles, Belgium, 2)BEAMS - Université Libre de Bruxelles, Belgium, 3)CoDE-SMG - Université Libre de Bruxelles, Belgium

A Message-Level Monitoring Protocol for QoS Flows in NoCs
Leonel Tedesco, Thiago Rosa, Fernando Moraes
PUCRS, Brazil

H.264/AVC Framework for Multi-Core Embedded Video Encoders
Tiago Dias[1], Nuno Roma[2], Leonel Sousa[2]
1) ISEL-PI Lisbon, INESC-ID Lisbon / IST-TU Lisbon, Portugal, 2) INESC-ID Lisbon / IST-TU Lisbon, Portugal

Low-power, High-throughput Deblocking Filter for H.264/AVC
Muhammad Nadeem[1], Stephan Wong[1], Georgi Kuzmanov[1], Ahsan Shabbir[2], Muhammad F. Nadeem[1], Fakhar Anjam[1]
1) TU Delft, The Netherlands, 2) TU Eindhoven, The Netherlands

Reducing Instruction Memory Energy Consumption by Use of the Instruction Buffer and After Scheduling Analysis
Vladimír Guzma, Teemu Pitkänen, Jarmo Takala
Tampere University of Technology, Finland

SESSION: Testing and Dependability
Location: Studio
Chair: Heikki Hurskainen, TUT

10:45 On-Line Dependability Enhancement of Multiprocessor SoCs by Resource Management
Timon D. Ter Braak[1], Stephen T. Burgess[2], Heikki Hurskainen[2], Hans G. Kerkhoff[1], Bart Vermeulen[3], Xiao Zhang[1]
1) University of Twente, The Netherlands, 2)Tampere University of Technology, Finland, 3) NXP, The Netherlands

11:05 Automatic Selection of Efficient Observability Points in Combinational Gate Level Circuits Using Particle Swarm Optimization
Amirali Ghofrani, Fatemeh Javaheri, Saeed Safari, Zainalabedin Navabi
University of Tehran, Iran

SESSION: Design Methodology
Location: Studio
Chair: Fabio Garzia, TUT

11:25 Correct and Energy-Efficient Design of SoCs: the H.264 Encoder Case Study
Adolf Abdallah[1], Abdoulaye Gamatie[2], Jean-Luc Dekeyser[1]
1) LIFL/USTL and INRIA, France, 2) LIFL/CNRS and INRIA, France

11:45 Interconnect Routing of Embedded FPGAs Using Standard VLSI Routing Tools
Thomas Coenen, Jochen Schleifer, Oliver Weiß, Tobias G. Noll
RWTH Aachen University, Germany

12:05 Heap Access Optimizations for a Hardware-Accelerated Java Virtual Machine
Joonas Tyystjärvi[1], Tero Säntti[2], Juha Plosila[3]
1) Turku Centre for Computer Science, Finland, 2) Department of Information Technology, University of Turku, Finland, 3) Academy of Finland, Research Council for Natural Sciences and Engineering

SESSION: Sensor Networks and Neural Networks
Location: Rondo
Chair: Erno Salminen, TUT

11:25 Hybrid On-Chip Clocking for Sensor Nodes
Spencer Kellis, Nathaniel Gaskin, Bennion Redd, Richard Brown
University of Utah, USA

11:45 Program Image Dissemination Protocol for Low-energy Multihop Wireless Sensor Networks
Lasse Määttä, Jukka Suhonen, Teemu Laukkarinen, Timo Hämäläinen, Marko Hännikäinen
Tampere University of Technology, Finland

12:05 EMBRACE-SysC for Analysis of NoC-based Spiking Neural Network Architectures
Sandeep Pande[1], Fearghal Morgan[1], Seamus Cawley[1], Brian McGinley[1], Snaider Carrillo[2], Liam McDaid[2], Jim Harkin[2]
1) National University of Ireland, Galway, Ireland 2) University of Ulster, UK

SESSION: Lunch
Location: Restaurant Fuuga

12:25 – 13:30

SESSION: Invited 5
Location: Studio
Chair: Jari Nurmi, TUT

13:30 MULTIPROCESSOR SYSTEM AND SOFTWARE DESIGN FOR DISTRIBUTED CONTROL APPLICATIONS
Samarjit Chakraborty, *TU Munich, Germany*

SESSION: Poster 4 and coffee
Location: Rondo

14:15 – 15:15
Useful-state Encoding: Network Control with Minimal Redundancy
Kris Heyrman and Peter Veelaert
Ghent University College, Belgium

A Digit-Set-Interleaved Radix-8 Division/Square Root Kernel for Double-Precision Floating-Point
Ingo Rust and Tobias G. Noll
RWTH Aachen University, Germany

Exploiting Control Management to Accelerate Radix-4 FFT on a Reconfigurable Platform
Waqar Hussain, Fabio Garzia, Jari Nurmi
Tampere University of Technology, Finland

Design and Implementation of an OS-CFAR Processor Based on a New Rank Order Filtering Algorithm
Zulfiqar Ali[1], Ali Arshad[1], Umair Razzaq[1], Sawaira Sana[2], Abdul Haseeb Ahmed[2], Abdullah Harris[3]
1) Irtiqa Technologies, Pakistan, 2)University of Michigan, Ann Arbor, USA,
3) Aalto University of Technology, Finland

SESSION: Architecture Analysis and Optimization
Location: Studio
Chair: Tapani Ahonen, TUT

15:15 Optimized Communication Architecture of MPSoCs with a Hardware Scheduler: A System View
Diandian Zhang[1], Han Zhang[1], Jeronimo Castrillon[1], Torsten Kempf[1], Gerd Ascheid[1], Rainer Leupers[1], Bart Vanthournout[2]
1) RWTH Aachen, Germany, 2) CoWare NV (Synopsys), Leuven, Belgium

15:35 LDPC Decoder Area, Timing, and Energy Models for Early Quantitative Hardware Cost Estimates
Matthias Korb and Tobias G. Noll
RWTH Aachen University, Germany

15:55 Power Emulation Based DVFS Efficiency Investigations for Embedded Systems
Andreas Genser[1], Christian Bachmann[1], Christian Steger[1], Reinhold Weiss[1], Josef Haid[2]
1) Graz University of Technology, Austria, 2) Infineon Technologies Austria AG

SESSION: Invited 6
Location: Studio
Chair: Jari Nurmi, TUT

16:15 PHYSICAL DESIGN ISSUES IN MP-SOC
Fabio Campi, *STMicroelectronics, Italy*

SESSION: Closing of SoC 2010
Time: 17:00 – 17:15
Location: Studio

SESSION: Ice-hockey Tappara vs. TPS
Time: 18:00 - 21:00
Location: Hakametsä Ice Hall

SESSION: Farewell Supper
Time: 21:00 - 23:00
Location: Brewery Restaurant Plevna

SoC 2010 Tampere Hall September 29-30, 2010

General Chair's message

Welcome to Tampere – The SoC City!

This is the 12th annual SoC event organized in Tampere, following the tradition of the previous years by providing a high-level invited lecture program, scientific paper program, a small exhibit, industrial program track, panel discussion, appealing social events – and reasonable amounts of coffee (as again pointed out in this program leaflet). In the scientific program we have selected 17 oral presentations and 17 posters from the quality paper submissions. This year the special theme is Embedded Multicore/Multiprocessor Computing Platforms. This is shown especially in invited talks and in the tutorial.

This year the tutorial was organized jointly with CRISP EU-project and GETA doctoral school. The topic was Dependable Hardware and Software for Embedded Multicore Computing Platforms, delivered by a number of professionals in this field.

The International Symposium on System-on-Chip has become The Place for the industry and academics in the SoC field to meet each others in a casual atmosphere. I hope that the presentations and all the informal discussions during the breaks and in the social events will inspire each of you in doing research and development towards more successful Systems-on-Chip.

Thanks to the numerous people who have contributed to the success of this event.

Next year the SoC symposium will take place on October 4-5 with a tutorial on October 3. The location will be exactly the same, mark your calendars and keep watching the details at **http://soc.cs.tut.fi/ -** and, by the way, we will be co-located with Conference on Design and Architectures for Signal and Image Processing DASIP 2011 taking place on the same week here. To follow up that, see **http://www.ecsi.org/dasip**

See you in Tampere also next year!

Prof. Jari Nurmi
General Chairman
SoC 2010