SoC 2011
International Symposium on System-on-Chip

Tampere Hall, Yliopistonkatu 55

Tampere, Finland, Nov 1-2, 2011

The 13th Annual SoC Event in Tampere

Organized by Department of Computer Systems, Tampere University of Technology.

Technical co-sponsorship by IEEE Circuits and Systems Society.

Financial sponsors: Nokia, Renesas Mobile, GETA, TISE, and IEEE Finland Section.

TAMPERE UNIVERSITY OF TECHNOLOGY

IEEE

Venue

Tampere Hall was inaugurated in 1990 and is the largest congress and concert centre in Scandinavia. Its modern architecture and integral works of art make Tampere Hall a sight worth seeing in itself. Tampere Hall is located on the edge of Sorsapuisto Park, beside Sorsalampi duck pond, within a short walking distance of the city centre.

Tampere – the SoC city – is situated in the heart of beautiful Finnish Lakeland. The banks of the Tammerkoski rapids still feature old traditional industrial buildings which have now been converted to house pleasant restaurants, pubs or high-tech companies. Tampere is also a city of theatres, arts, sciences, sport and modern industrial culture.

Premises

The oral presentations will take place in room “Studio” and poster sessions and coffee in the adjacent room “Rondo”. Plenary talks with DASIP are also in Studio.

List of exhibiting entities

- CREMA coarse-grain reconfigurable computing platform
- Groundhow benchmarking suite
- KACTUS open-source design tools
- NINESILICA open-source computing platform
- SYSMODEL system-level modelling project
- TTA open-source design tools

INTERNATIONAL SYMPOSIUM ON SYSTEM-ON-CHIP 2011

Tampere Hall, Tampere, Finland, November 1-2, 2011

PROGRAMME AT A GLANCE

MONDAY Oct. 31
09:00 - 17:00 Tutorial on System Level Modeling
17:00 – 17:30 Early registration (Tampere Hall)

TUESDAY Nov. 1
08:00 – 09:00 Registration
09:00 – 09:15 Opening
09:15 – 10:00 Invited1 (Axel Jantsch, KTH)
10:00 – 10:30 Coffee
10:30 – 11:30 SESSION: System-Level Design Flow and Methodology
11:30 – 12:30 SESSION: Processor Architectures
12:30 – 13:30 Lunch
13:30 – 14:15 Invited2 (Leandro Soares Indrusiak, U York)
14:15 – 15:15 SESSION: SoC Design and Analysis Methods
15:15 – 16:00 Posters Coffee
16:00 – 16:45 Invited3 (Jan Madsen, DTU)
16:45 – 18:00 Panel discussion: System-Level Design Challenges

18:00 – 18:45 Reception in poster hall

WEDNESDAY Nov. 2
09:00 – 09:20 DASIP 2011 opening
09:20 – 10:05 Invited4 (Yves Leduc, U Nice) – plenary with DASIP 2011
10:05 – 11:00 Posters Coffee
11:00 – 12:20 SESSION: Network-on-Chip and Inter-Chip Communications
12:20 – 14:00 Lunch
14:00 – 14:45 Invited5 (Toshihiro Hattori, Renesas Mobile) – plenary with DASIP 2011
14:45 – 15:25 SESSION: Software Tools
15:30 – 16:00 DASIP posters Coffee
16:00 – 16:45 Invited6 (Patricia Derler, UC Berkeley) – plenary with DASIP 2011
16:45 – 17:00 Closing SoC 2011

19:30 – 22:00 Banquet (Finlayson Palace) – plenary with DASIP 2011

SoC 2011 Detailed Program Schedule

TUESDAY Nov. 1

SESSION: Opening
Location: Studio

09:00 WELCOME TO SOC 2011
Jari Nurmi, Tampere University of Technology

SESSION: Keynote
Location: Studio
Chair: Jari Nurmi, TUT

09:15 **3D Integration of NoC-based Systems**
Axel Jantsch, KTH, Sweden

SESSION: Coffee
Location: Rondo

10:00 – 10:30

SESSION: System-Level Design Flow and Methodology
Location: Studio
Chair: Erno Salminen, TUT

10:30 **Analyzing Layer-2 Performance and Scalability in System-Level Performance Simulation**
Subayal Khan[1], Jukka Saastamoinen[1], Mikko Majanen Majanen[1], Jari Nurmi[2]
[1]VTT Technical Research Centre of Finland, [2]Tampere University of Technology

10:50 **Moonrake Chip - GALS Demonstrator in 40 nm CMOS Technology**
Milos Krstic[1], Xin Fan[1], Eckhard Grass[1], Luca Benini[2], M. R. Kakoee[2], Christoph Heer[3], Birgit Sanders[3], Alessandro Strano[4], Davide Bertozzi[4]
[1]IHP, [2]University of Bologna, [3]Intel Mobile Communications, [4]University of Ferrara

11:10 **Analyzing Synchronous Dataflow Scenarios for Dynamic Software-defined Radio Applications**
Firew Siyoum[1], Marc Geilen[1], Orlando Moreira[2], Rick Nas[2], Henk Corporaal[1]
[1]Eindhoven University of Technology, [2]ST-Ericsson Eindhoven

SESSION: Processor Architectures
Location: Studio
Chair: Olli Vainio, TUT

11:30 **A Hybrid Model of Speculative Execution and Scout Threading for Auto-Memoization Processor**
Tomoki IKEGAYA[1], Ryosuke ODA[1], Tatsuhiro YAMADA[1], Tomoaki TSUMURA[1], Hiroshi MATSUO[1], Yasuhiko NAKASHIMA[2]
[1]Nagoya Inst. of Tech., [2]Nara Inst. of Sci. and Tech.

11:50 **Customizable Datapath Integrated Lock Unit**
Pekka Jääskeläinen, Erno Salminen, Otto Esko, Jarmo Takala
Tampere University of Technology.

12:10 **Exploring Instruction caching strategies for tightly-coupled shared-memory clusters**
Daniele Bortolotti, Francesco Paterna, Christian Pinto, Andrea Marongiu, Martino Ruggiero, Luca Benini
University of Bologna - DEIS

SESSION: Lunch
Location: Restaurant Fuuga

12:30 – 13:30

SESSION: Invited 2
Location: Studio
Chair: Sanna Määttä, TUT

13:30 **Fast and accurate system-level model of a NoC-based MPSoC supporting real-time applications**
Leandro Soares Indrusiak, *University of York, UK*

SESSION: SoC Design and Analysis Methods
Location: Studio
Chair: Sanna Määttä, TUT

14:15 **Static Analysis Method for Deadlock Detection in SystemC Designs**
Mikhail Moiseev[1], Alexey Zakharov[1], Ilya Klotchkov[2], Sergey Salishev[2]
[1]SPbSPU, [2]Intel Labs

14:35 **SAMOSA: Scratchpad Aware Mapping Of Streaming Applications**
Zubair Wadood Bhatti[1], Davy Preuveneers[1], Narasinga Rao Miniskar[2], Roel Wuyts[2], Yolande Berbers[1]
[1]K.U.Leuven, [2]IMEC

14:55 **Hybrid System Level Power Consumption Estimation for FPGA-Based MPSoC**
Santhosh Kumar Rethinagir[1], Rabie ben Atitallah[2], Jean-Luc Dekeyser[3]
[1]INRIA, [2]Univ.Valenciennes, [3]Univ. Lille

SESSION: Posters and coffee
Location: Rondo

15:15 – 16:00

OpenCL Implementation of Cholesky Matrix Decomposition
Claudio Brunelli, Eero Aho, Heikki Berg
Nokia

Low-power Arithmetic Unit for DSP Applications
Mehdi Modaressi[1], Hossein Nikonia[2], Amir-Hossein Jahangir[1]
[1]Sharif University of Technology, [2]Tehran University

Co-designs of Parallel Rijndael
Issam Damaj
American University of Kuwait

A Set of Traffic Models for Network-on-Chip Benchmarking
Esko Pekkarinen, Lasse Lehtonen, Erno Salminen, Timo D. Hämäläinen
Tampere University of Technology

Effects of Loop Unrolling and Use of Instruction Buffer on Processor Energy Consumption
Vladimír Guzma, Teemu Pitkänen, Jarmo Takala
Tampere University of Technology

Product data management using IP-XACT
Erno Salminen, Timo D. Hämäläinen, Marko Hännikäinen
Tampere University of Technology

Increasing Energy Efficiency of Automotive E/E-Architectures with Intelligent Communication Controllers for FlexRay
Christoph Schmutzler[1], Abdallah Lakhtel[1], Martin Simons[1], Jürgen Becker[2]
[1]Daimler AG, [2]Karlsruhe Institute of Technology, ITIV

An Automatic Experimental Set-Up for Robustness Analysis of Designs Implemented on SRAM FPGAs
Uli Kretzschmar, Armando Astarloa, Jesús Lázaro, Jaime Jiménez, Aitzol Zuloaga
Universidad del Pais Vasco UPV/EHU

A Coarse-Grained Reconfigurable Protocol Processor
Mohammad Badawi and Ahmed Hemani
Royal Institute of Technology, Stockholm, Sweden

moviTest: A Test Environment Dedicated to Multi-Core Embedded Architectures
Teodor Tite[1], Adelina Vig[1], Nicolae Olteanu[2], Cristian Cuna[2]
[1]University "Politehnica" of Timisoara, Department of Computer and Software Engineering, Timisoara, Romania, [2]Movidius SRL, Tools Department, Timisoara, Romania

SESSION: Invited 3
Location: Studio
Chair: Jari Nurmi, TUT

16:00 **Addressing Risk Management during Design Space Exploration**
Jan Madsen, *DTU, Denmark*

SESSION: Panel Discussion: System-Level Design Challenges
Time: 16:45 – 18:00
Location: Studio

SESSION: Reception
Location: Rondo

18:00 – 18:45

WEDNESDAY Nov. 2

SESSION: DASIP 2011 Opening
Location: Studio

09:00 WELCOME TO DASIP 2011
Tapani Ahonen and Jari Nurmi, *Tampere University of Technology, Finland*

SESSION: Invited 4
Location: Studio
Chair: Jari Nurmi, TUT

09:20 **SoC, MPSoC, RSoC, ... , Design Challenges, The Industrial Point of View**
Yves Leduc, *University of Nice, France*

SESSION: Posters and coffee
Location: Rondo

10:05 – 11:00

All the posters on display for DASIP participants, too.

SESSION: Network-on-Chip and Inter-Chip Communications
Location: Studio
Chair: Peeter Ellervee, Tallinn University of Technology

11:00 **Mismatch Characterization of High-Speed NoC Links using Asynchronous Sub-sampling**
Sebastian Höppner, Dennis Walter, Georg Ellguth, Renè Schüffny
TU Dresden

11:20 **Impact of Proactive Temperature Management on Performance of Networks-on-Chip**
Tim Wegner, Martin Gag, Dirk Timmermann
University of Rostock

11:40 **Bringing Network-on-Chip Links to 45nm**
Marco Ferraresi, Giuseppina Gobbo, Daniele Ludovici, Davide Bertozzi
University of Ferrara

12:00 **Synchronizing Distributed State Machines in a Coarse Grain Reconfigurable Architecture**
Omer Malik and Ahmed Hemani
Royal Institute of Technology - KTH

SESSION: Lunch
Location: Restaurant Fuuga

12:20 - 14:00

SESSION ThuAm4: Invited 5
Location: Studio
Chair: Tapani Ahonen, TUT

14:00 **Design challenges in SoCs for mobile devices**
Toshihiro Hattori, *Renesas Mobile Corporation, Japan*

SESSION: Software Tools
Location: Studio
Chair: Tapani Ahonen, TUT

14:45 **Automatic Calibration of Streaming Applications for Software Mapping Exploration**
Weihua Sheng, Stefan Schürmans, Maximilian Odendahl, Rainer Leupers, Gerd Ascheid
RWTH Aachen University

15:05 **Building a RTOS for MPSoC Dataflow Programming**
Yaset Oliva[1], Maxime Pelcat[1], Jean-Francois Nezan[1], Jean-Christophe Prévotet[1], Aridhi Slaheddine[2]
[1]IETR/INSA Rennes, [2]Texas Instruments

SESSION: DASIP posters and coffee
Location: Rondo

15:30 – 16:00

DASIP poster session.

SESSION: Invited 6
Location: Studio
Chair: Jari Nurmi, TUT

16:00 **Heterogeneous Concurrent Modeling and Design in Java**
Patricia Derler, *UC Berkeley, USA*

SESSION: Closing
Time: 16:45 – 17:00
Location: Studio

BANQUET
Time: 19:30 - 22:00
Location: (restaurant Finlayson Palace)

SoC 2011 Tampere Hall November 1-2, 2011
General Chair's message

Welcome to Tampere – The SoC City!

This is the 13th annual SoC event organized in Tampere, following the tradition of the previous years by providing a high-level invited lecture program, scientific paper program, a small exhibit, industrial program track, panel discussion, appealing social events – and reasonable amounts of coffee for fueling discussions. In the scientific program we have selected 15 oral presentations and 10 posters from the quality paper submissions. This year we are co-located with the Conference on Design and Architectures for Signal and Image Processing (DASIP) on November 2-4. This is shown in plenary invited and poster/coffee sessions and a joint banquet between the events. The participants of SoC and DASIP represent over 20 different nationalities.

This year we can also enjoy of a tutorial on System-Level Modelling, organized jointly with the SYSMODEL project and two national doctoral programmes, TISE and GETA. The instructors come from the project partners and other major international players in the system modelling field.

The International Symposium on System-on-Chip has become The Place for the industry and academics in the SoC field to meet each others in a casual atmosphere. I hope that the presentations and all the informal discussions during the breaks and in the social events will inspire each of you in doing research and development towards more successful Systems-on-Chip.

Thanks to the numerous people who have contributed to the success of this event.

Next year the SoC symposium will take place on October 11-12 with a tutorial on October 10. We will be co-located with Embedded Systems Week which will bring the opportunity for SoC visitors to participate also a number of other conferences and workshops during the whole week from October 7 to October 12. The location for SoC will be exactly the same, mark your calendars and keep watching the details at **http://soc.cs.tut.fi/**

See you in Tampere also next year!

Prof. Jari Nurmi
General Chairman
SoC 2011