SoC 2014
International Symposium on System-on-Chip

Tampere Hall, Yliopistonkatu 55

Tampere, Finland, Oct 28-29, 2014

The 16th Annual SoC Event in Tampere

Organized by Department of Electronics and Communications Engineering, Tampere University of Technology.

Technical co-sponsorship by IEEE Circuits and Systems Society.

Financial sponsors: Federation of Finnish Learned Societies, IEEE CASS Distinguished Lecturer Program, IEEE Finland Section.

TAMPERE UNIVERSITY OF TECHNOLOGY

IEEE

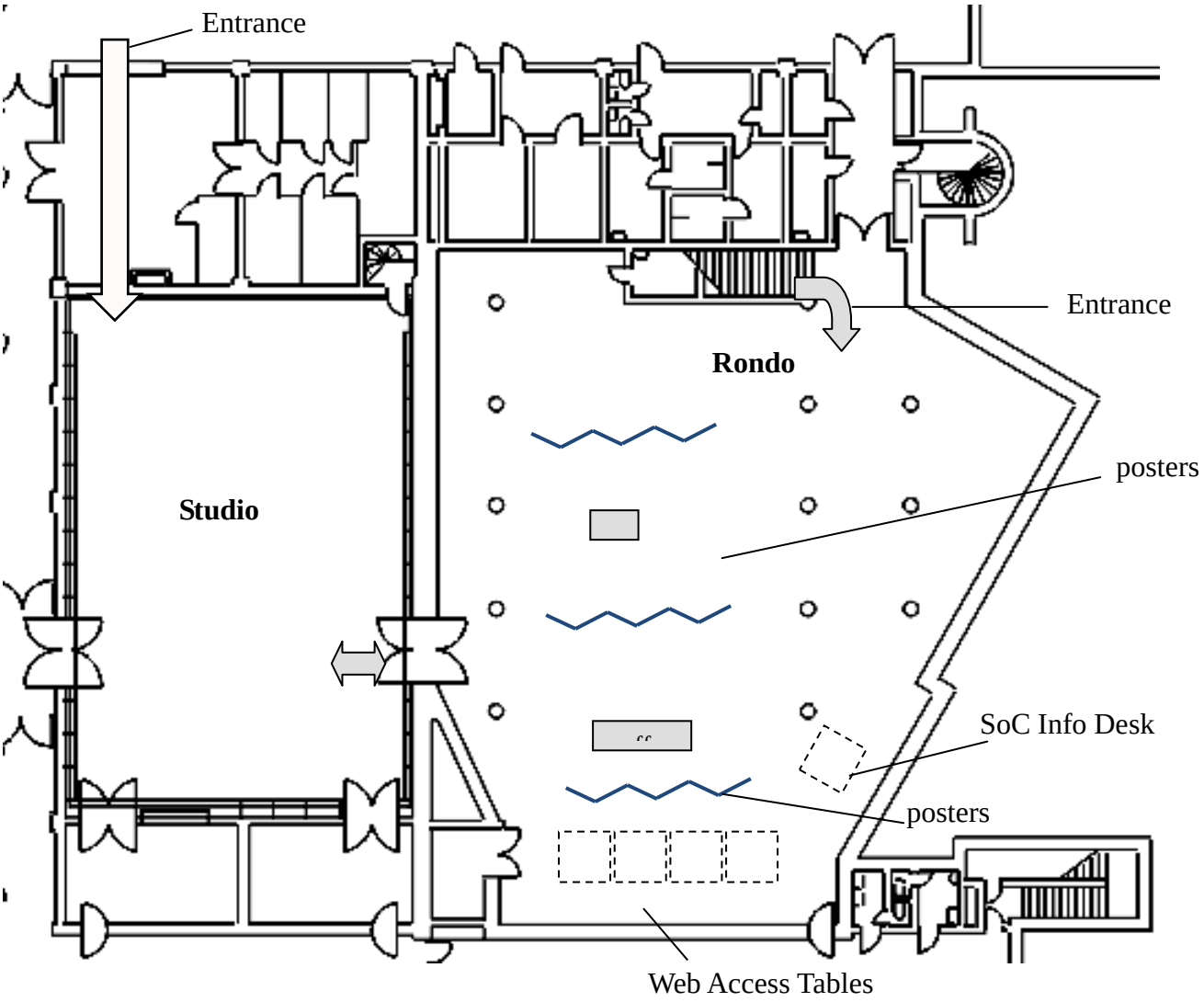
Venue

Tampere Hall was inaugurated in 1990 and is the largest congress and concert centre in Scandinavia. Its modern architecture and integral works of art make Tampere Hall a sight worth seeing in itself. Tampere Hall is located on the edge of Sorsapuisto Park, beside Sorsalampi duck pond, within a short walking distance of the city centre.

Tampere – the SoC city – is situated in the heart of beautiful Finnish Lakeland. The banks of the Tammerkoski rapids still feature old traditional industrial buildings which have now been converted to house pleasant restaurants, pubs or high-tech companies. Tampere is also a city of theatres, arts, sciences, sport and modern industrial culture.

Premises

The oral presentations will take place in room “Studio” and poster sessions and coffee in the adjacent room “Rondo”.



INTERNATIONAL SYMPOSIUM ON SYSTEM-ON-CHIP 2014

Tampere Hall, Tampere, Finland, October 28-29, 2014

PROGRAMME AT A GLANCE

Sunday Oct. 26
13:30 - 17:00 Tutorial on Physical Design Automation of Transistor Networks

Monday Oct. 27
09:00 – 17:10 NORCHIP 2014 programme
13:30 - 17:00 Tutorial on Software-Defined Electronics: a new research field for CASS

Tuesday Oct. 28
09:00 – 09:15 Opening
09:15 – 10:00 Keynote 1 (Ricardo Reis, UFRGS, Brazil)
10:00 – 10:40 SESSION: Special Applications | Norchip: Time-to-digital converters
10:40 – 11:25 Norchip Posters Coffee
11:25 – 12:25 SESSION: Design Analysis | Norchip: Analog circuits
12:25 – 13:30 Lunch
13:30 – 14:15 Keynote 2 (Geza Kolumban, Pázmány Péter Catholic University, Hungary)
14:15 – 14:30 NORCHIP & SOC 2015 Announcement
14:30 – 15:30 SESSION: Data-path Optimizations
15:30 – 16:00 Coffee
16:00 – 17:00 SESSION: Physical Level Design Issues

17:30 – 18:00 Bus transport to ice-hockey
18:30 – 20:45 Ice-hockey Tappara vs. JYP
21:00 – 23:00 Supper in brewery restaurant Plevna

Wednesday Oct. 29
09:00 – 09:45 Invited 3 (Hank Hoffmann, University of Chicago)
09:45 – 10:25 SESSION: Alternative Computing Concepts
10:25 – 11:00 Coffee
11:00 – 12:20 SESSION: Design Methodology
12:20 – 13:30 Lunch
13:30 – 14:15 Inivited 4 (Vianney Lapôtre, UBS, France)
14:15 – 15:20 SPECIAL SESSION: Multicore and Manycore Architectures, Applications and Platforms
15:20 – 15:40 Coffee
15:40 – 16:40 SPECIAL SESSION: Advances in High Performance Reconfigurable Architectures
16:40 – 16:50 Closing SoC 2014

19:00 – 22:00 Farewell Banquet in Ristorante Como

SoC 2014 Detailed Programme Schedule

Tuesday Oct. 28

Registration
Location: in front of Studio
08:30 – 09:00

SESSION: Opening
Location: Studio
09:00 **WELCOME TO SOC 2014**
Jari Nurmi, Tampere University of Technology, Finland

SESSION: Keynote 1
Location: Studio
Chair: Jari Nurmi, TUT, Finland
09:15 **Challenges for Electronics Design in the Nano-Scale**
Ricardo Reis, Universidade Federal do Rio Grande do Sul, Brazil

SESSION: Special Applications
Location: Studio
Chair: Geza Kolumban, Pázmány Péter Catholic University, Hungary
10:00 **System on Chip Design of a Linear System Solver**
Bucek, Jiri; Kubalik, Pavel; Lorencz, Robert; Zahradnicky, Tomas
Czech Technical University in Prague, Czech Republic
10:20 **Adaptive Runtime Management of Heterogeneous MPSoCs: Analysis, Acceleration and Silicon Prototype (PhD forum submission)**
Arnold, Oliver; Fettweis, Gerhard; TU Dresden, Germany

SESSION: Coffee break
Location: Rondo
10:40 – 11:25 Coffee and NORCHIP posters

SESSION: Design Analysis
Location: Studio
Chair: Claudio Brunelli, Microsoft, Finland
11:25 **A Cycle-Accurate Network-on-Chip Simulator with Support for Abstract Task Graph**
Joseph, Jan Moritz; Pionteck, Thilo; Universität zu Lübeck, Germany
11:45 **Fast Memory Region: 3D DRAM memory concept evaluated for JPEG2000 algorithm**
Schoenberger, Alex; Hofmann, Klaus; TU Darmstadt, Germany
12:05 **A Transaction-Level Framework for Design-Space Exploration of Hardware-Enhanced Operating Systems**
Gregorek, Daniel; García-Ortiz, Alberto; University of Bremen, Germany

SESSION: Lunch
Location: Restaurant Fuuga
12:25 – 13:30

SESSION: Keynote 2
Location: Studio
Chair: Jari Nurmi, TUT, Finland

13:30 **New approach for design and implementation of future communications systems**
Geza Kolumban, Pázmány Péter Catholic University, Hungary

SESSION: NORCHIP & SoC 2015 Announcement
Location: Studio

14:15 – 14:30

SESSION: Data-Path Optimizations
Location: Studio
Chair: Erno Salminen, TUT, Finland

14:30 **Optimal Data Path Widths for Energy- and Area-efficient Max-Log-MAP Based LTE Turbo Decoders**
Broich, Martin; Noll, Tobias G.; RWTH Aachen University, Germany

14:50 **Energy-efficiency of floating-point and fixed-point SIMD cores for MIMO processing systems**
Günther, Daniel; Bytyn, Andreas; Leupers, Rainer; Ascheid, Gerd
RWTH Aachen University, Germany

15:10 **L2_ISA++: Instruction Set Architecture Extensions for 4G and LTE-Advanced MPSoCs**
Arnold, Oliver; Neumärker, Felix; Fettweis, Gerhard; TU Dresden, Germany

SESSION: Coffee break
Location: Rondo

15:30 - 16:00

SESSION: Physical Level Design Issues
Location: Studio
Chair: Peeter Ellervee, Tallinn University of Technology, Estonia

16:00 **Limits of gate-level power estimation considering real delay effects and glitches**
Meixner, Michael; Noll, Tobias G.; RWTH Aachen University, Germany

16:20 **Unbalanced Buffer Tree Synthesis to Suppress Ground Bounce for Fine-grain Power Gating**
Usami, Kimiyoshi [1]; Miyauchi, Makoto [1]; Kudo, Masaru [1]; Takagi, Kazumitsu [1]; Amano, Hideharu [2]; Namiki, Mitaro [3]; Kondo, Masaaki [4]; Nakamura, Hiroshi [4]
1) Shibaura Institute of Technology, Japan; 2) Keio University, Japan; 3) Tokyo University of Agriculture and Technology, Japan; 4) The University of Tokyo, Japan

16:40 **Keyed Logic BIST for Trojan Detection in SoC**
Dubrova, Elena [1]; Näslund, Mats [2]; Carlsson, Gunnar [2]; Smeets, Ben [2]
1) KTH, Sweden 2) Ericsson AB, Sweden

17:00 End of session

17:30 Bus transport

SESSION: Ice-Hockey
Location: Hakametsä Ice Hall

18:30 – 20:45

Bus transport after the game

SESSION: Supper
Location: Brewery Restaurant Plevna, Itäinenkatu 8

21:00 – 23:00

WEDNESDAY Oct. 29

SESSION: Invited 3
Location: Studio
Chair: Waqar Hussain, TUT, Finland

09:00 **Untapped Opportunities for Manycore Communication Optimization**
Hank Hoffmann, University of Chicago, IL, USA

SESSION: Alternative Computing Concepts
Location: Studio
Chair: Jari Nurmi, TUT, Finland

09:45 **Soft-Core eFPGA for Smart Power Applications**
Cuppini, Matteo [1]; Mucci, Claudio [2]; Franchi Scarselli, Eleonora [1]; Canegallo, Roberto [2]
1) University of Bologna, Italy; 2) STMicroelectronics, Agrate Brianza, Italy

10:05 **An Implementation of Auto-Memoization Mechanism on ARM-based Superscalar Processor**
Shibata, Yuuki [1]; Tsumura, Takanori [1]; Tsumura, Tomoaki [1]; Nakashima, Yasuhiko [2]
1) Nagoya Institute of Technology, Japan
2) Nara Institute of Science and Technology, Japan

SESSION: Coffee break
Location: Rondo
10:25 - 11:00

SESSION: Design Methodology
Location: Studio
Chair: Tapani Ahonen, TUT, Finland

11:00 **WOKE: A novel workflow model editor**
Salminen, Erno; Honkonen, Mikko; Matilainen, Lauri; Hämäläinen, Timo D.
Tampere University of Technology, Finland

11:20 **Early Power-aware Design Space Exploration for Embedded Systems: MPEG-2 Case Study**
Ben Abdallah, Feriel [1]; Trabelsi, Chiraz [2]; Ben Atitallah, Rabie [2]; Abed, Mourad [2]
1) Institut Mines-Telecom, Telecom ParisTech, France
2) University of Valenciennes, France

11:40 **Gamification of System-on-Chip Design**
Hämäläinen, Timo D.; Salminen, Erno; Tampere University of Technology, Finland

12:00 **Formal Verification of Circuit-Switched Network on Chip (NoC) Architectures using SPIN**
Zaman, Anam; Hasan, Osman; National University of Science and Technology, Pakistan

SESSION: Lunch
Location: Restaurant Fuuga
12:20 – 13:30

SESSION: Invited 4
Location: Studio
Chair: Waqar Hussain, TUT, Finland

13:30 **A Dynamically Reconfigurable Multi-ASIP Architecture for Multi-Standard and Multi-Mode Turbo Decoding**
Vianney Lapôtre, Université de Bretagne-Sud, France

SPECIAL SESSION: Multicore and Manycore Architectures, Applications and Platforms
Location: Studio
Chair: Waqar Hussain, TUT, Finland

14:00 **A Many-Core Hardware Acceleration Platform for Short Read Mapping Problems Using Distributed Memory Interface with 3D-stacked Architecture**
Liu, Pei; KTH, Sweden

14:20 **Implementation of Multicore Communications API**
Virtanen, Janne; Matilainen, Lauri; Salminen, Erno; Hämäläinen, Timo D.; TUT, Finland

14:40 **I/O Virtualization Utilizing an Efficient Hardware System-level Memory**
Kornaros, George; Harteros, Kostantinos; Christoforakis, Ioannis; Astrinaki, Maria
Technological Educational Institute of Crete, Greece

15:00 **A Communication Model and Partitioning Algorithm for Streaming Applications for an Embedded MPSoC**
Kelly, Wayne [1]; Flaßkamp, Martin [2]; Sievers, Gregor [2]; Ax, Johannes [2]; Chen, Jianing [1]; Klarhorst, Christian [2]; Ragg, Christoph [2]; Jungeblut, Thorsten [2]; Sorensen, Andrew [1]
1) Queensland University of Technology, Brisbane, Australia
2) Bielefeld University, Germany

SESSION: Coffee break
Location: Rondo

15:20– 15:40

SPECIAL SESSION: Advances in High Performance Reconfigurable Architectures
Location: Studio
Chair: Tapani Ahonen, TUT, Finland

15:40 **Constraint-Driven Frequency Scaling in a Coarse Grain Reconfigurable Array**
Hussain, Waqar [1]; Hoffmann, Henry [2]; Ahonen, Tapani [1]; Nurmi, Jari [1]
1) TUT, Finland; 2) University of Chigago, IL, USA

16:00 **A Reconfigurable MapReduce Accelerator for multi-core all-programmable SoCs**
Kachris, Christoforos; Sirakoulis, Georgios; Soudris, Dimitrios
Democritus University of Thrace, Greece

16:20 **Parallel and Distributed Simulation of networked Multi-Core Systems**
Wehner, Philipp; Göhringer, Diana; Ruhr-University Bochum, Germany

SESSION: Closing
Location: Studio

16:40 – 16:50

SESSION: Farewell Banquet
Location: Ristorante Como, Hämeenkatu 7

19:00 – 22:00

General Chair's message

Welcome to Tampere – The SoC City!

This is the 16th annual SoC event organized in Tampere, following the tradition of the previous years by providing a high-level invited lectures, scientific paper programme, and appealing social events – and reasonable amounts of coffee for fueling discussions. In the scientific program we have selected 24 oral presentations from the quality paper submissions.

The International Symposium on System-on-Chip has become The Place for the industry and academics in the SoC field to meet each others in a casual atmosphere. I hope that the presentations and all the informal discussions during the breaks and in the social events will inspire each of you in doing research and development towards more successful Systems-on-Chip.

Thanks to the numerous people who have contributed to the success of this event.

This year SoC symposium is co-located and interleaved with the Nordic Microelectronics Conference NORCHIP, which allows for mingling with colleagues from adjacent fields. Both conferences are technically co-sponsored by IEEE Circuits and Systems Society. Both events are also thankful for the support from the Federation of Finnish Learned Societies. For next year, there might be some major changes in the format of SoC coming, so keep watching the details at **http://soc.cs.tut.fi/** while working on the research for your next paper in SoC proceedings.

See you in SoC also next year!

Prof. Jari Nurmi
General Chair
SoC 2014